Compal Confidential

Model Name : BA41_HS
Compal Project Name : P4VC0
File Name : LA-7361P

Compal Confidential

BA41_HS(P4VC0) M/B Schematics Document

Intel Sandy Bridge Processor(ULV) with DDRIII + Cougar Point PCH
Nvidia N12P GV

2011-05-27

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2010/10/05	Deciphered Date	2011/10/5

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ZZZ
DAZ0J500100

ZZZ1 — SAM512M@ X76301BOL01 — 512M SAM(64Mx16)
ZZZ — SAM1G@ X76301BOL03 — 1G SAM(128Mx16)
ZZZ1 — HYN512M@ X76301BOL02 — 512M HYN(64Mx16)
ZZZ — HYN1G@ X76301BOL04 — 1G HYN(128Mx16)

UCPU1 — CPU2@ SA00004L940 — 1.5G
UCPU1 — CPU3@ SA00004N220 — 1.6G
UCPU1 — CPU4@ SA00004QZ40 — 1.3G I3
UCPU1 — CPU5@ SA00004RJ10 — 1.3G I5
UCPU1 — CPU6@ SA00004X010 — 1.6G i5
UCPU1 — CPU7@ SA00004VZ10 — 1.7G i5
UCPU1 — CPU8@ SA00004VY10 — 1.7G i7
UCPU1 — CPU9@ SA00004VW10 — 1.8G I7
UCPU1 — CPU10@ SA00005MX60 — 1.5G I3

Fan Control page 48

HDMI Conn. page 34
HDMI
Nvidia N12P GV page22~30
PEG(DIS) 100MHz PCI-E 2.0x16 5GT/s PER LANE
133MHz
Intel Sandy Bridge Processor ULV BGA1023 page 4~10
Memory BUS(DDRIII) Dual Channel
1.5V DDRIII 1066/1333
204pin DDRIII-SO-DIMM X2 BANK 0, 1, 2, 3 page 11,12

CRT Conn. page 33
CRT Mux page 33
CRT(VGA)
CRT(UMA)
LVDS Conn. page 32
LVDS Mux page 31
LVDS(VGA)
LVDS(UMA)

FDI x8 100MHz 2.7GT/s
DMI x4 100MHz 1GB/s x4

USB 2.0 conn x2 — USB port 0,1 on USB/B page 43
Bluetooth Conn — USB port 13 page 43
CMOS Camera — USB port 10 page 32
3G connector — USB port 9,12 on 3G/SIM page 39
USBx14 3.3V 48MHz

MINI Card x2 WLAN, WWAN page 38,39
port 2,3
PCI-Express x 8 (ARD PCIE2.0 2.5GT/s) 100MHz
SATA x 6 (GEN1 1.5GT/S ,GEN2 3GT/S) 100MHz
port 5 port 4 port 1 or 6

Intel Cougar Point-M PCH 989pin BGA page 13~21

HD Audio 3.3V 24MHz
SPI

WLAN Conn — USB port 8 page 38
eSATA Conn — USB port 4 page 35
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NEC uPD720200AF1 page 40
RTS5209-GR page 42
LAN(GbE) BCM57761 page 36
port 4 eSATA Conn. page 35
port 0 SATA HDD Conn. page 35
port 3 mSATA Conn. page 39
SPI ROM x1 page 13

USB 3.0 conn page 41
Card Reader Conn page 42
RJ45 page 37

LPC BUS 33MHz
ENE KB930 page 44
TPM SA19NP18ER28PVMK page 48

HDA Codec ALC271X page 46
Int. Speaker page 47
Phone Jack x 2 page 47

Touch Pad page 43
Int.KBD page 45
SPI ROM page 45

sub-board
LS7361P USB/B
LS7362P Function BTN/B
LS7363P Finger/B

RTC CKT. page 13
Power On/Off CKT. page 45
DC/DC Interface CKT. page 49,50
Power Circuit DC/DC page 51~60

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_PCH to +1.05VS_VCCP for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCPP to +1.05VS_PCH switched power rail for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT (R0.1)
Pre-DVT(R0.2)
DVT
PVT-1(R0.4)
PVT-2(R0.5)
Pre-MP

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & mSATA & BT & USB30 & USB20 Config

N12P-GS: GS@ OPTMIUS SKU: OPT@
N12P-GV: GV@ Non-OPTMIUS SKU: NOPT@
USB30 SKU: USB30@ 3G SKU: 3G@ & 3GPWR@
USB20 SKU: USB20@ mSATA SKU: mSATA@ & 3GPWR@
Combo Card SKU: COMBO@

BOM Config

UMA Only: CPU1@/3G@/3GPWR@/USB30@/UMA@/UMAO@/NOPT@
OPTIMUS(N12P-GV): CPU1@/3G@/3GPWR@/USB30@/UMA@/DIS@/SG@/OPT@/GV@
DIS Only(N12P-GV): CPU1@/3G@/3GPWR@/USB30@/DISO@/DIS@/NOPT@/GV@

VRAM P/N :
64*16
Samsung : SA00004GS10
Hynix : SA000041S40

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS MUX	SW@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
3G PWR side	3G PWR@
mSATA	mSATA@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
N12P-GS	GS@
N12P-GV	GV@
Combo card	COMBO@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
	UHCI1	2	USB3.0 colay USB2.0 Conn.
		3	
	UHCI2	4	E-SATA
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card 1(WLAN)
		9	3G/B(WWAN)
	UHCI5	10	Camera
		11	Finger Print
	UHCI6	12	3G/B(SIM Card)
		13	BlueTooth

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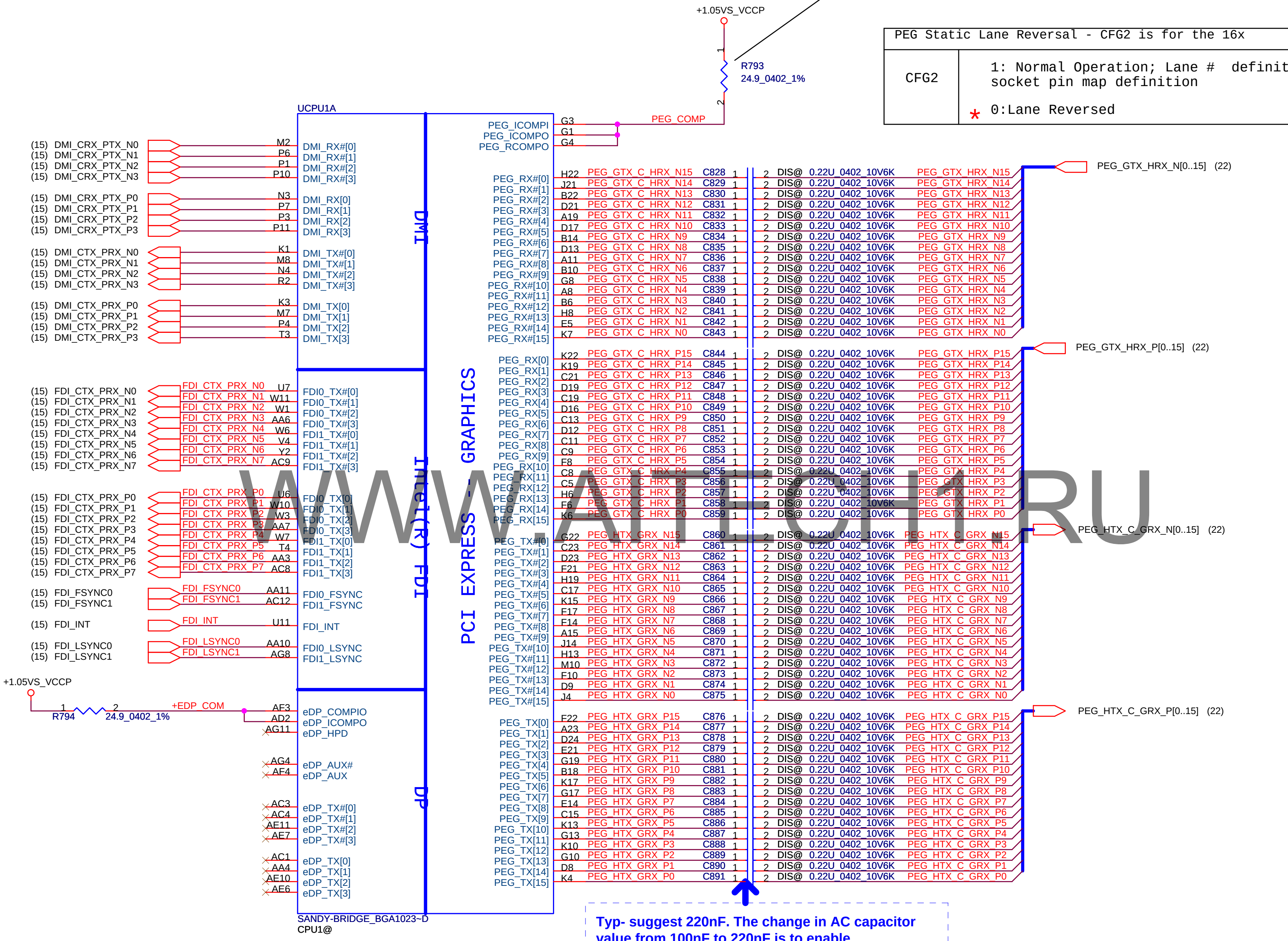
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

ULV type P/N is SA00004H960

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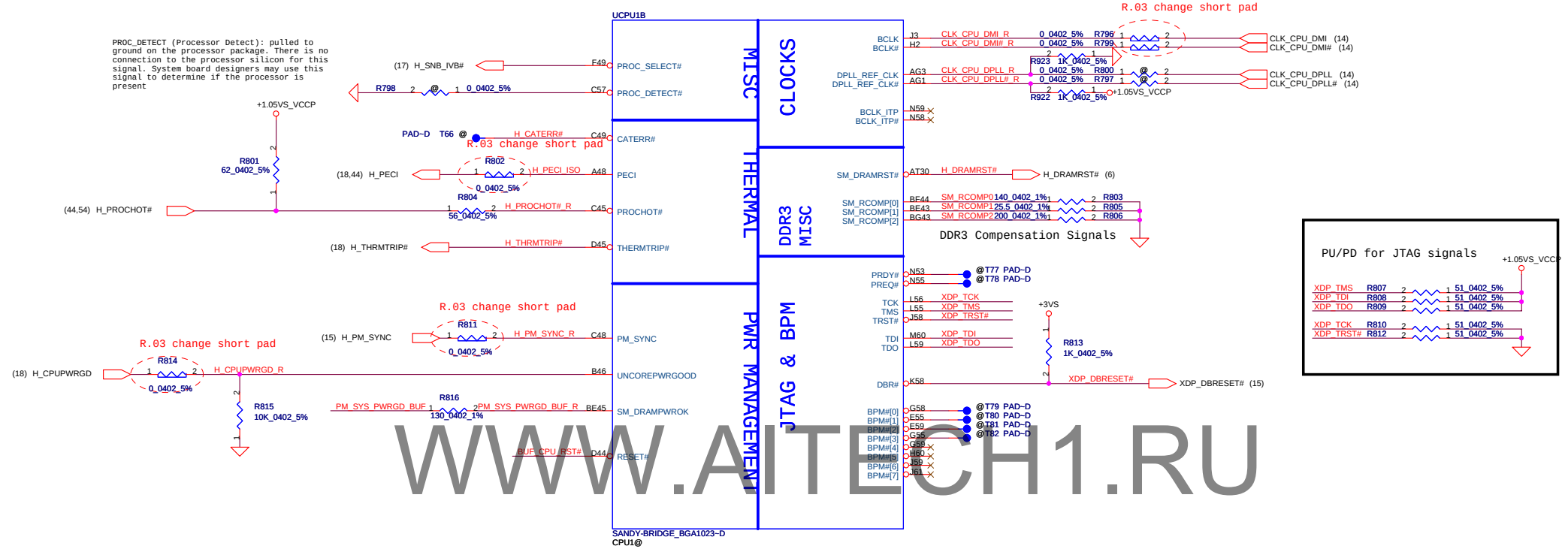

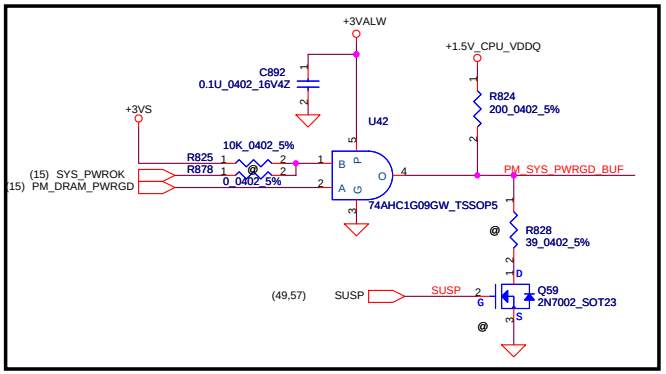

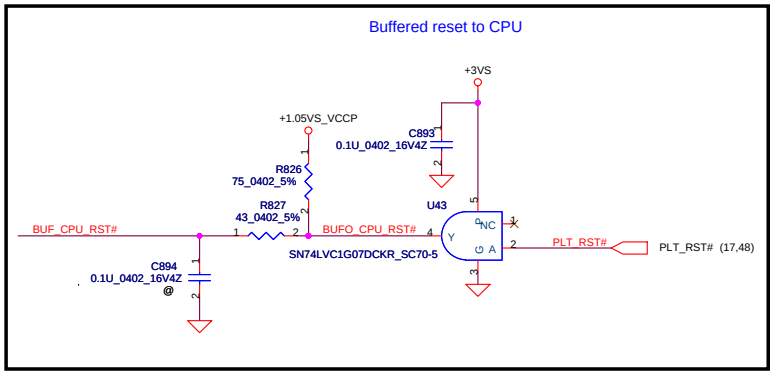

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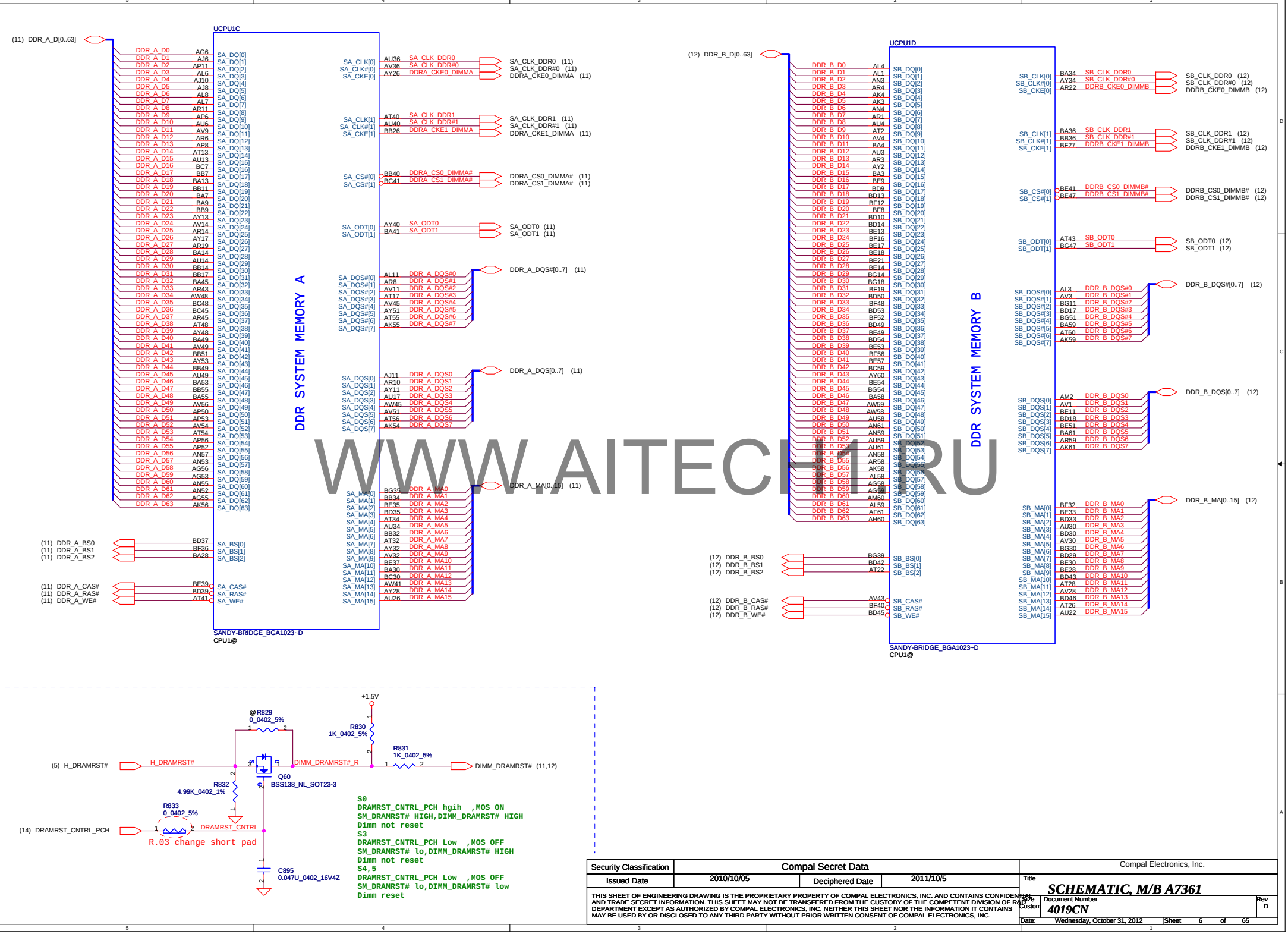

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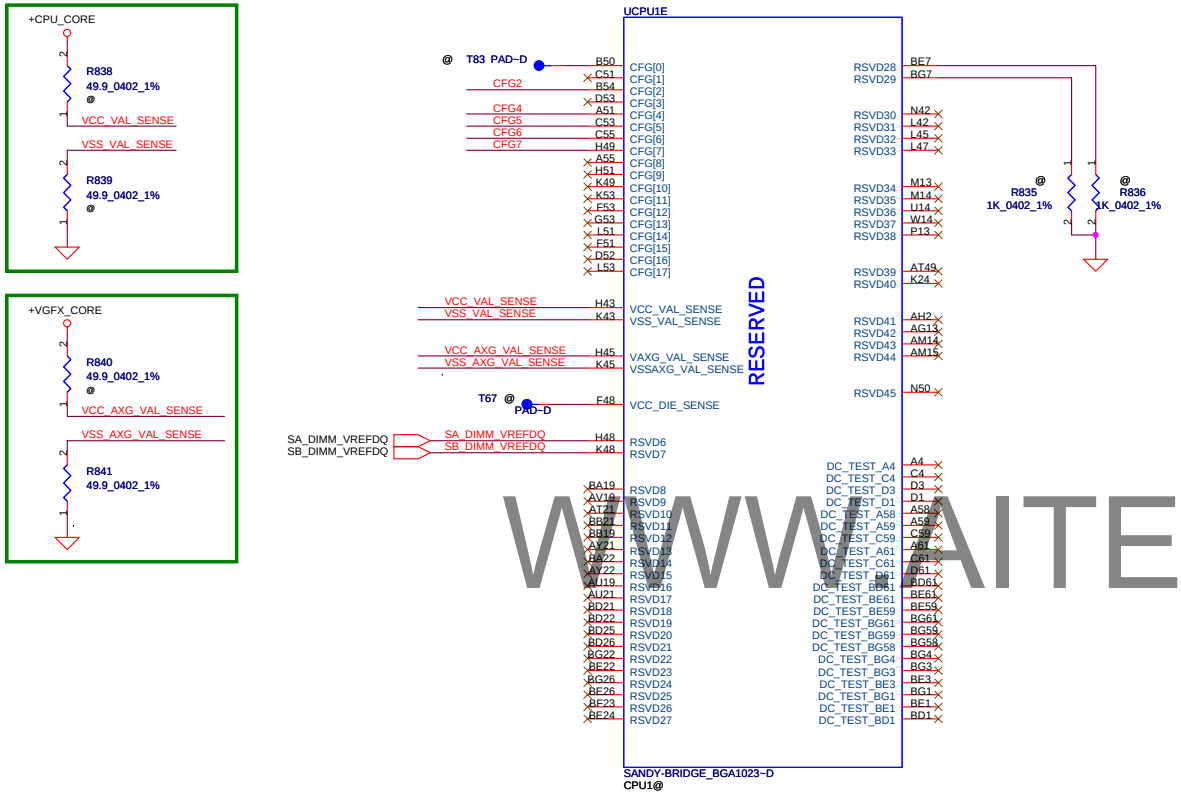
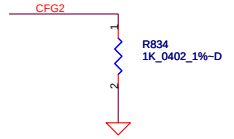
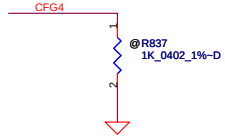
CFG Straps for Processor

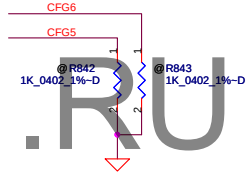




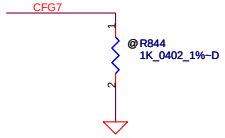
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition *0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 :(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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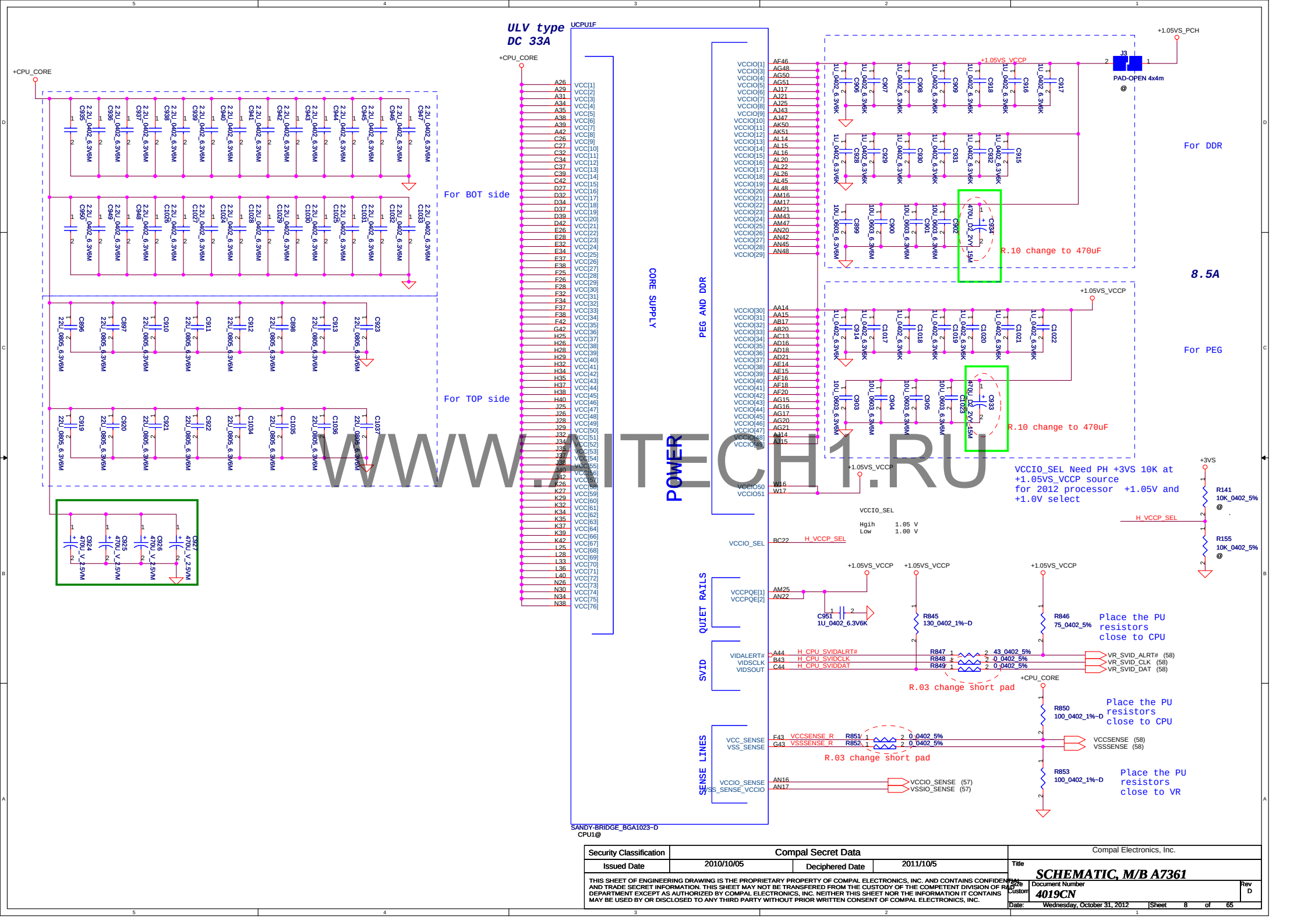

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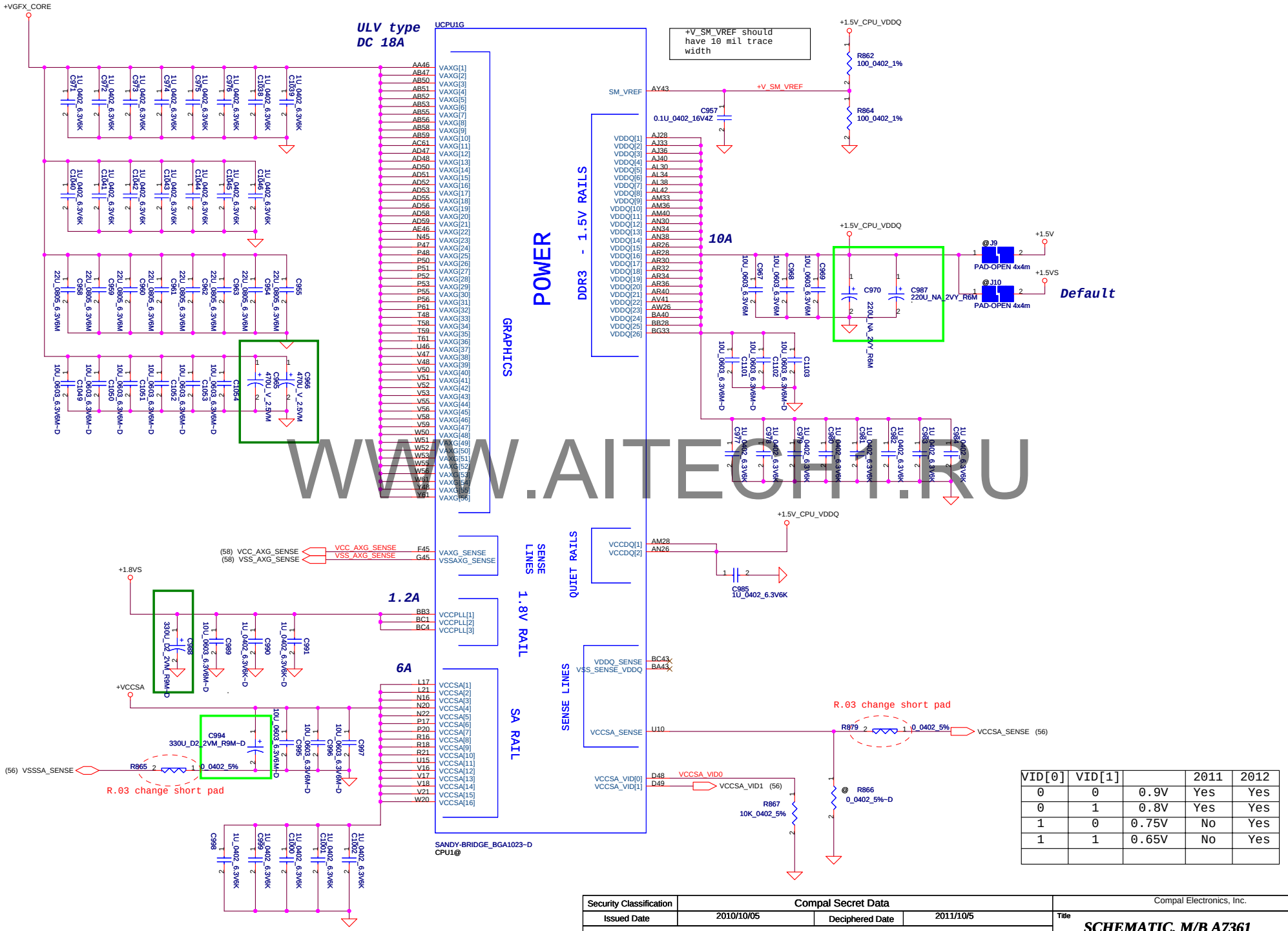

VID[0]	VID[1]		2011	2012
0	0	0.9V	Yes	Yes
0	1	0.8V	Yes	Yes
1	0	0.75V	No	Yes
1	1	0.65V	No	Yes

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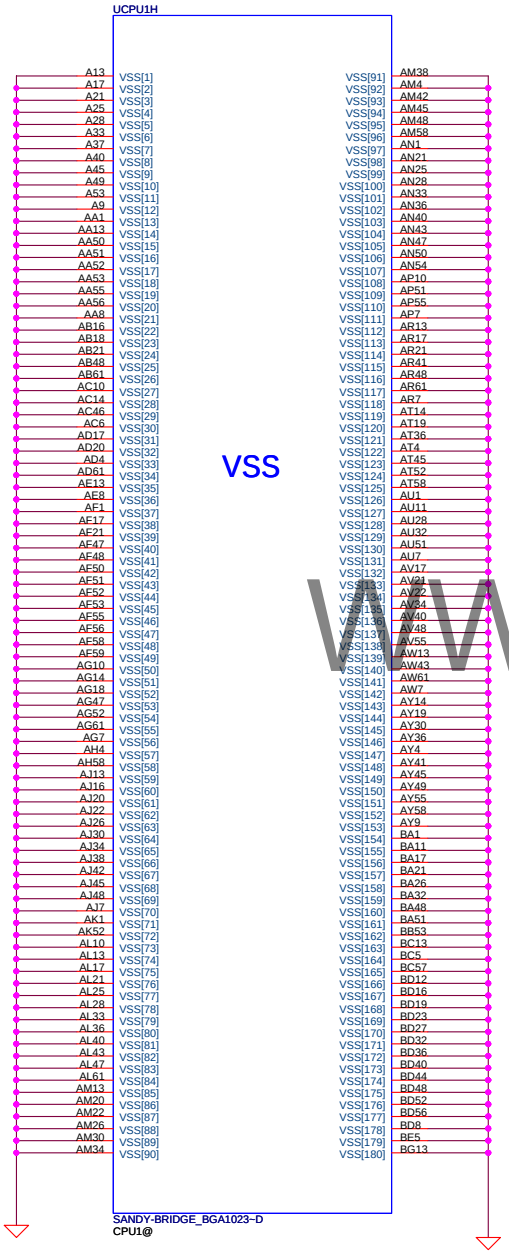

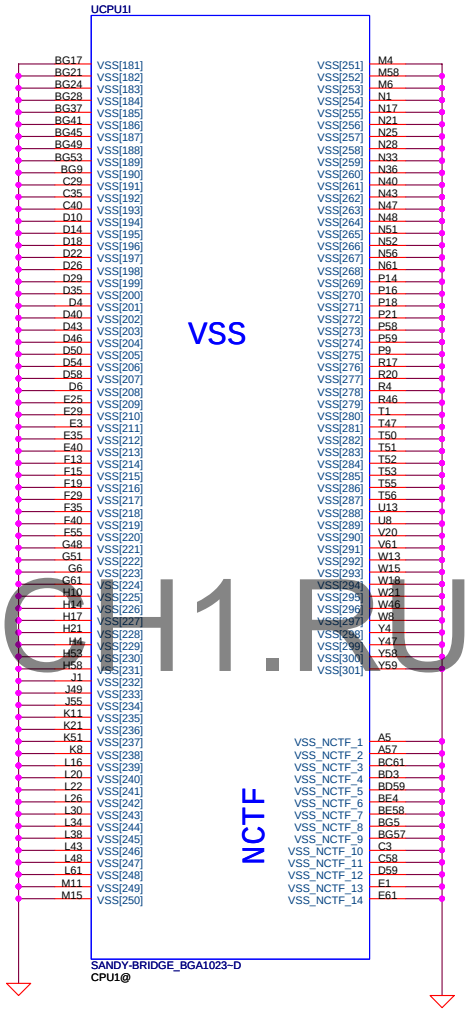

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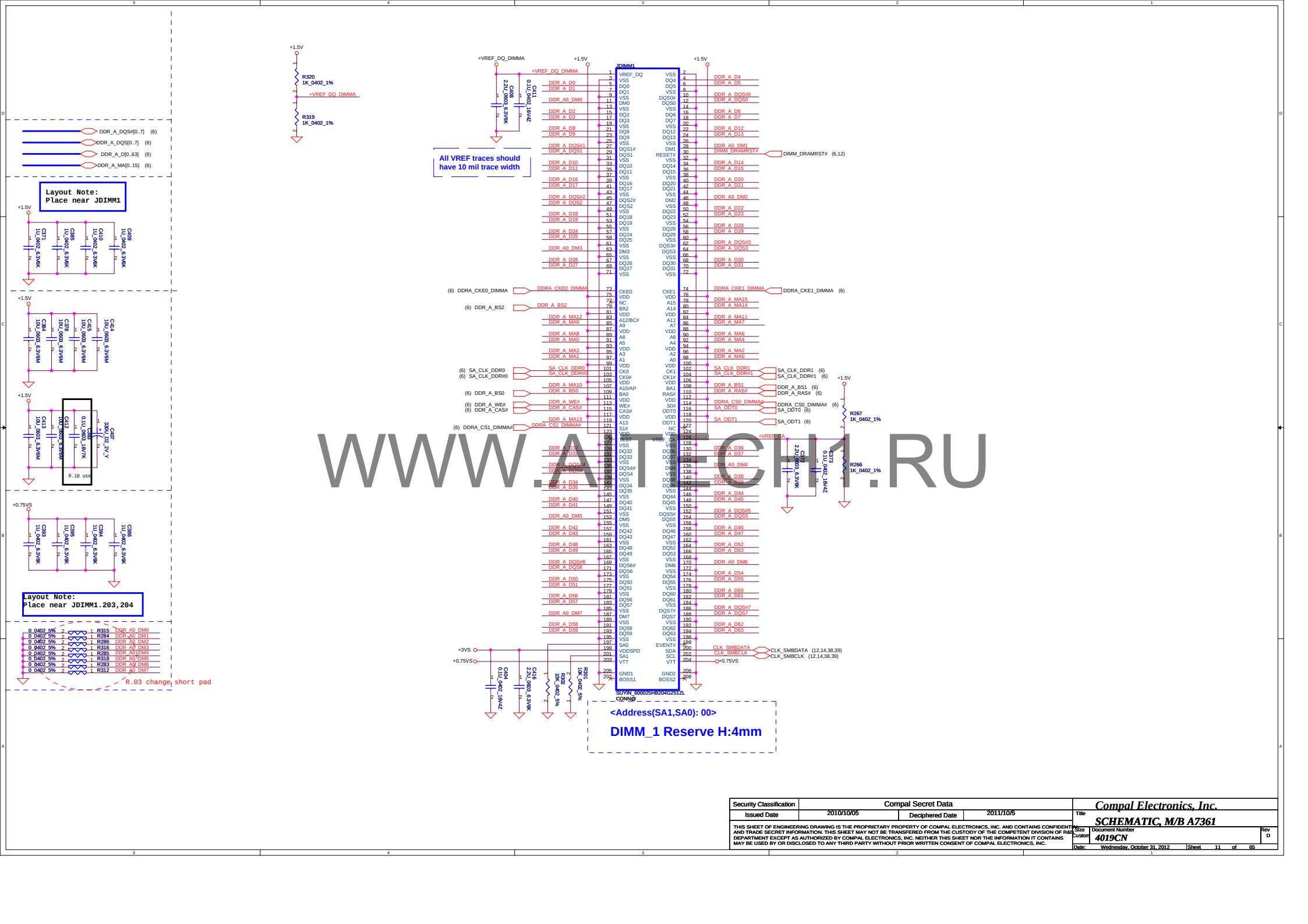

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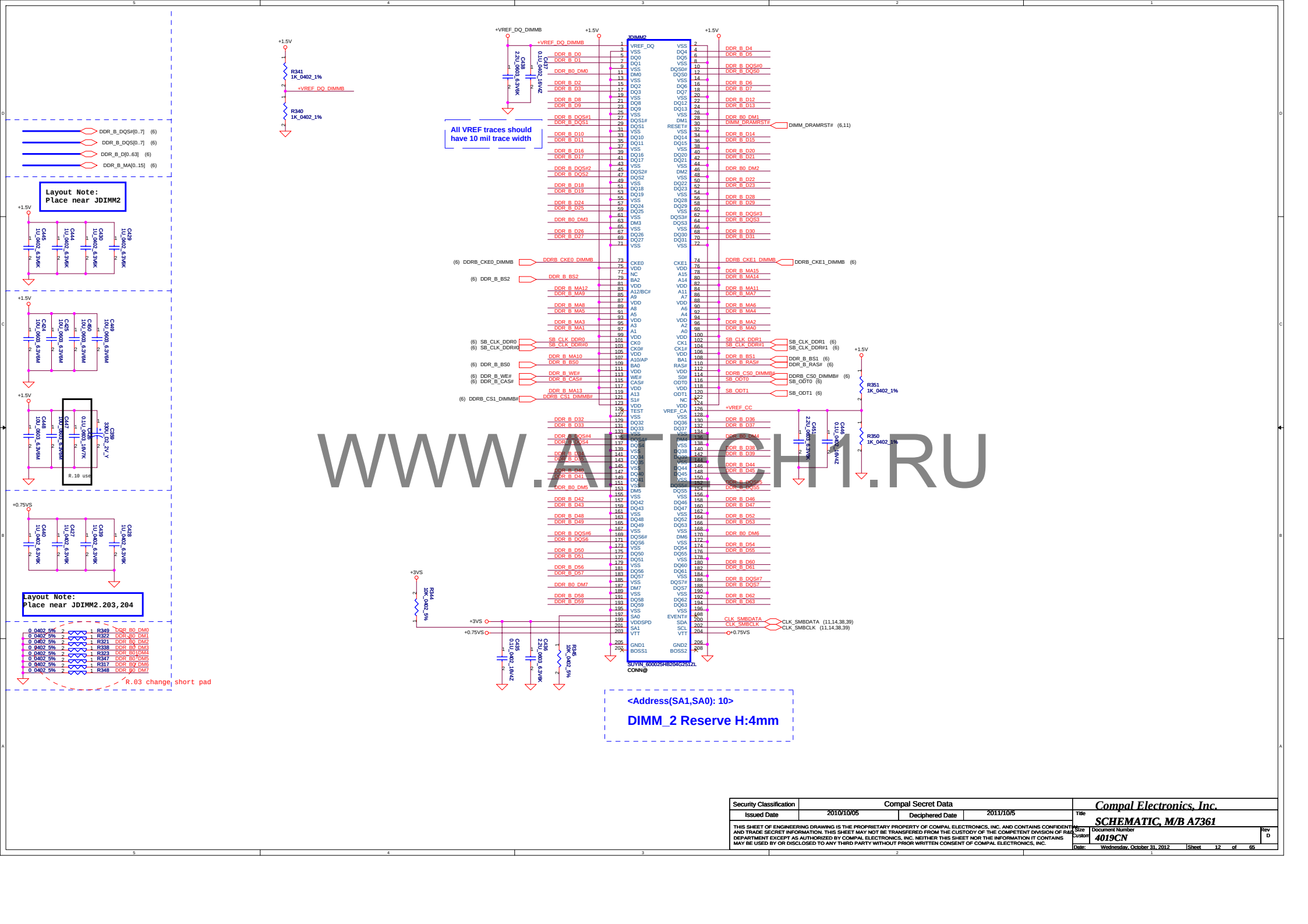

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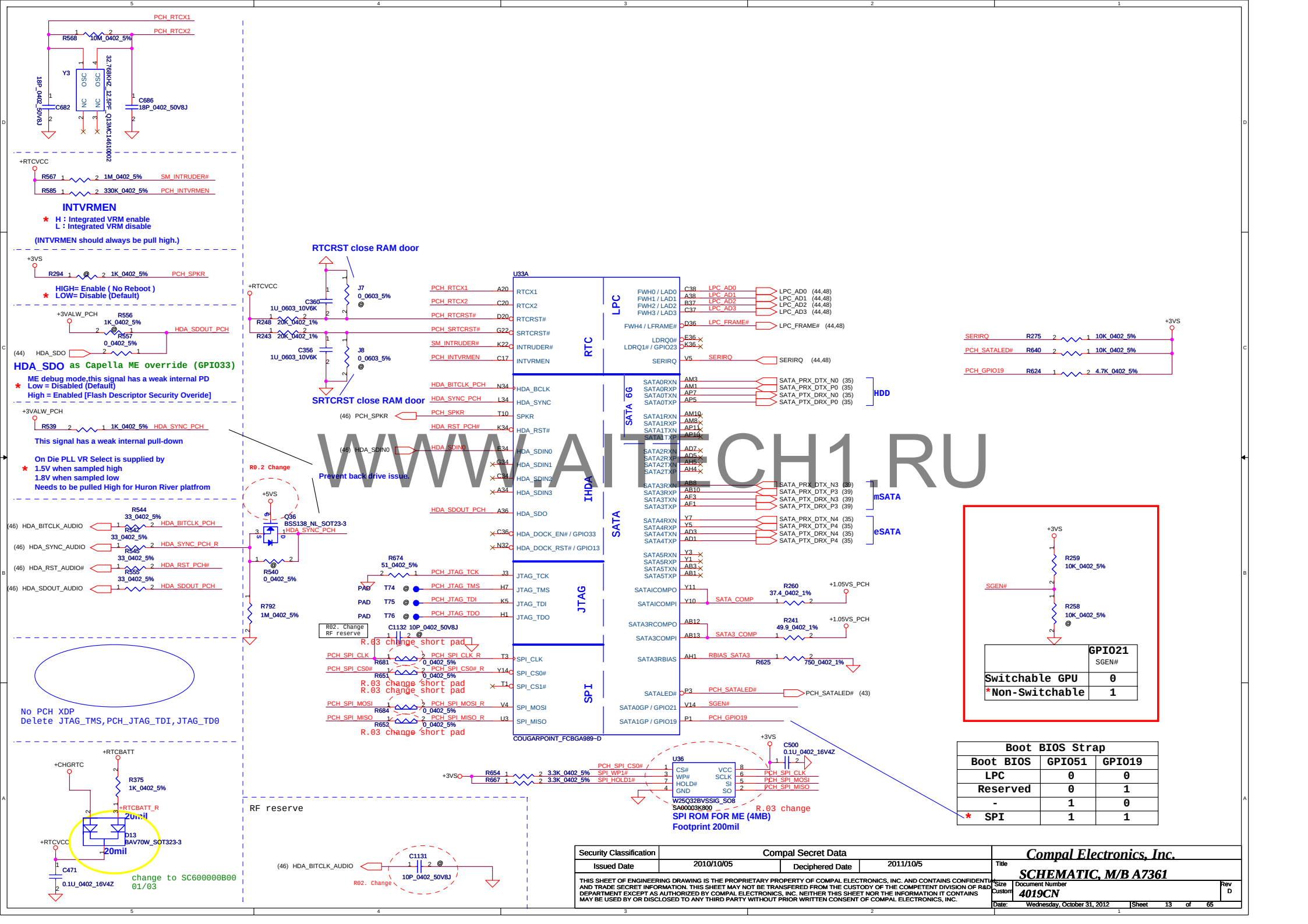

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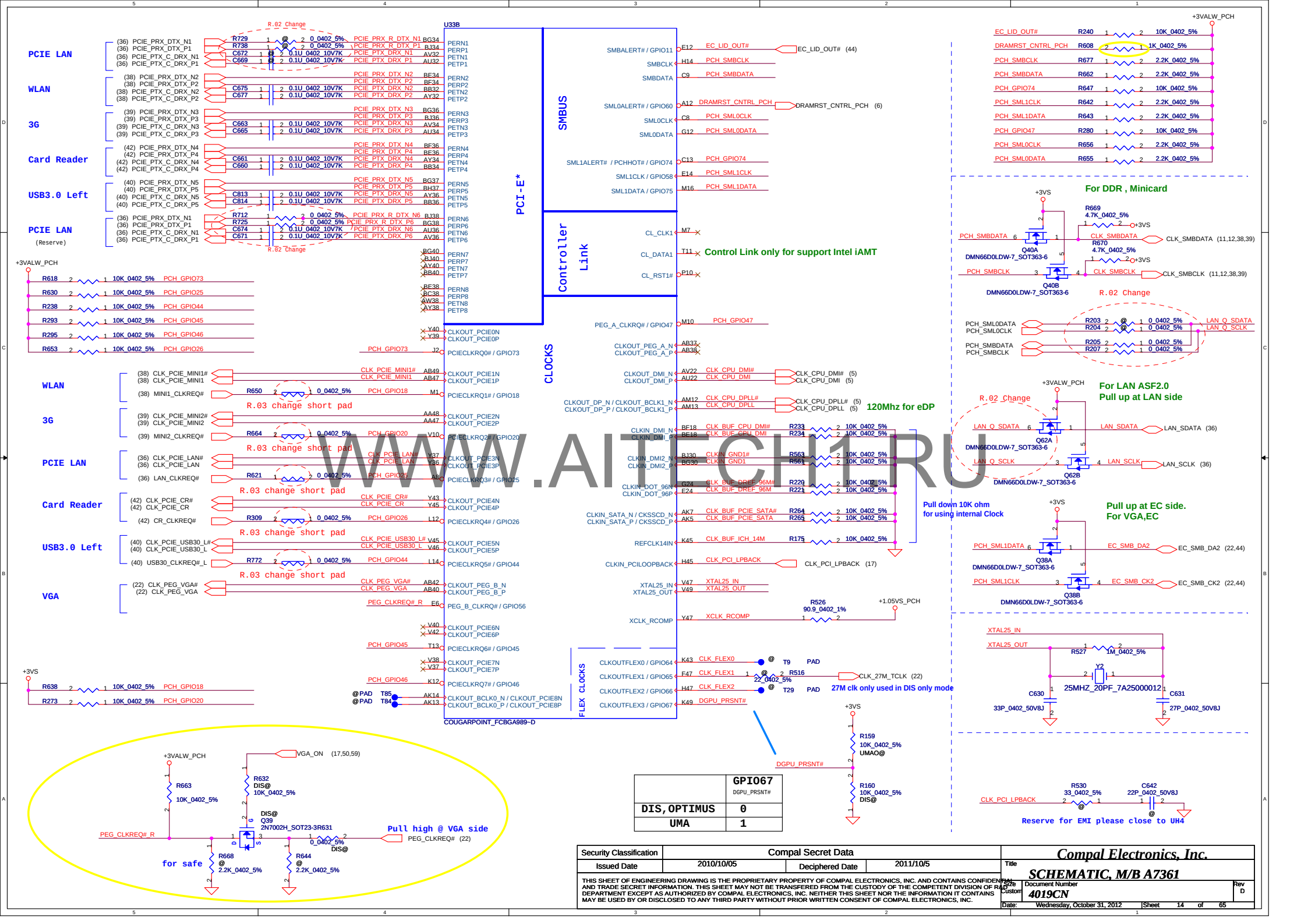

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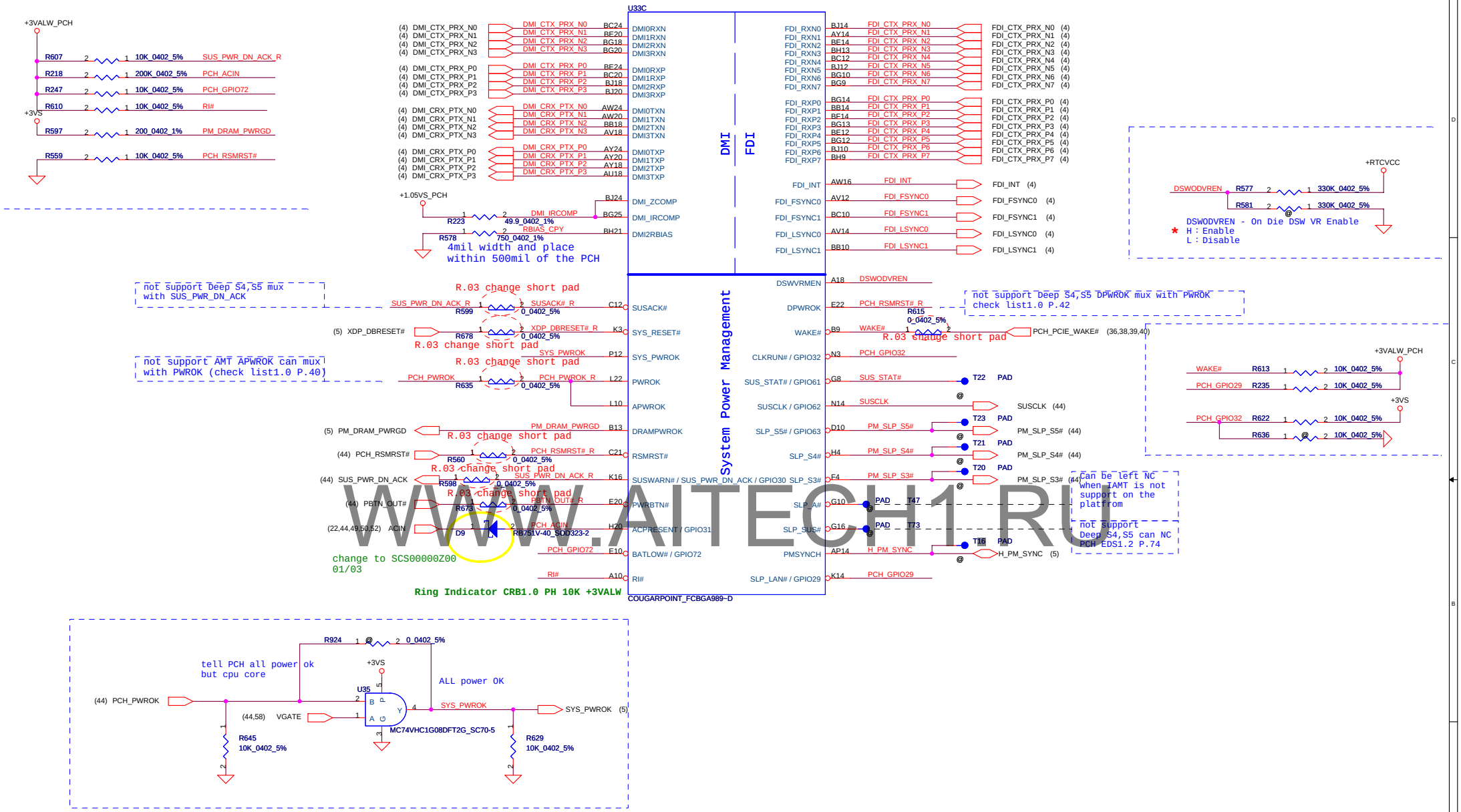

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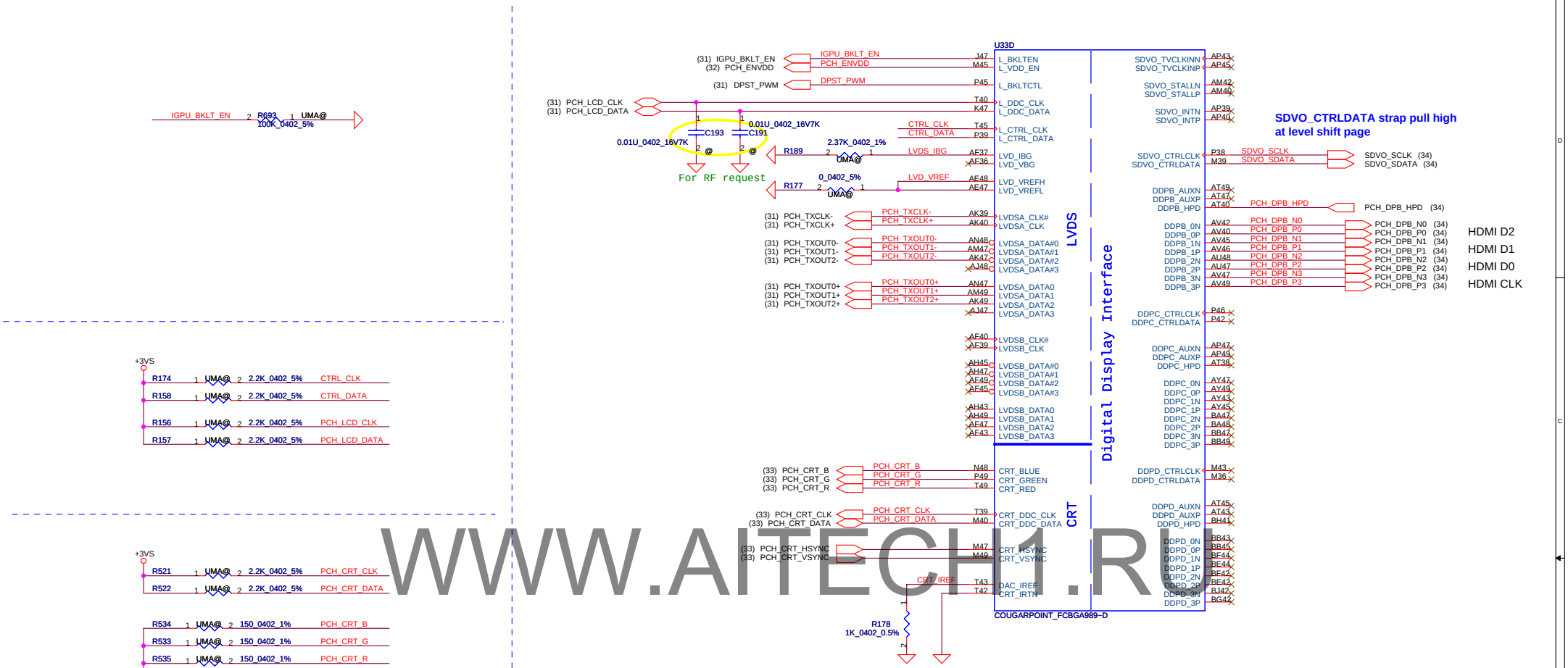

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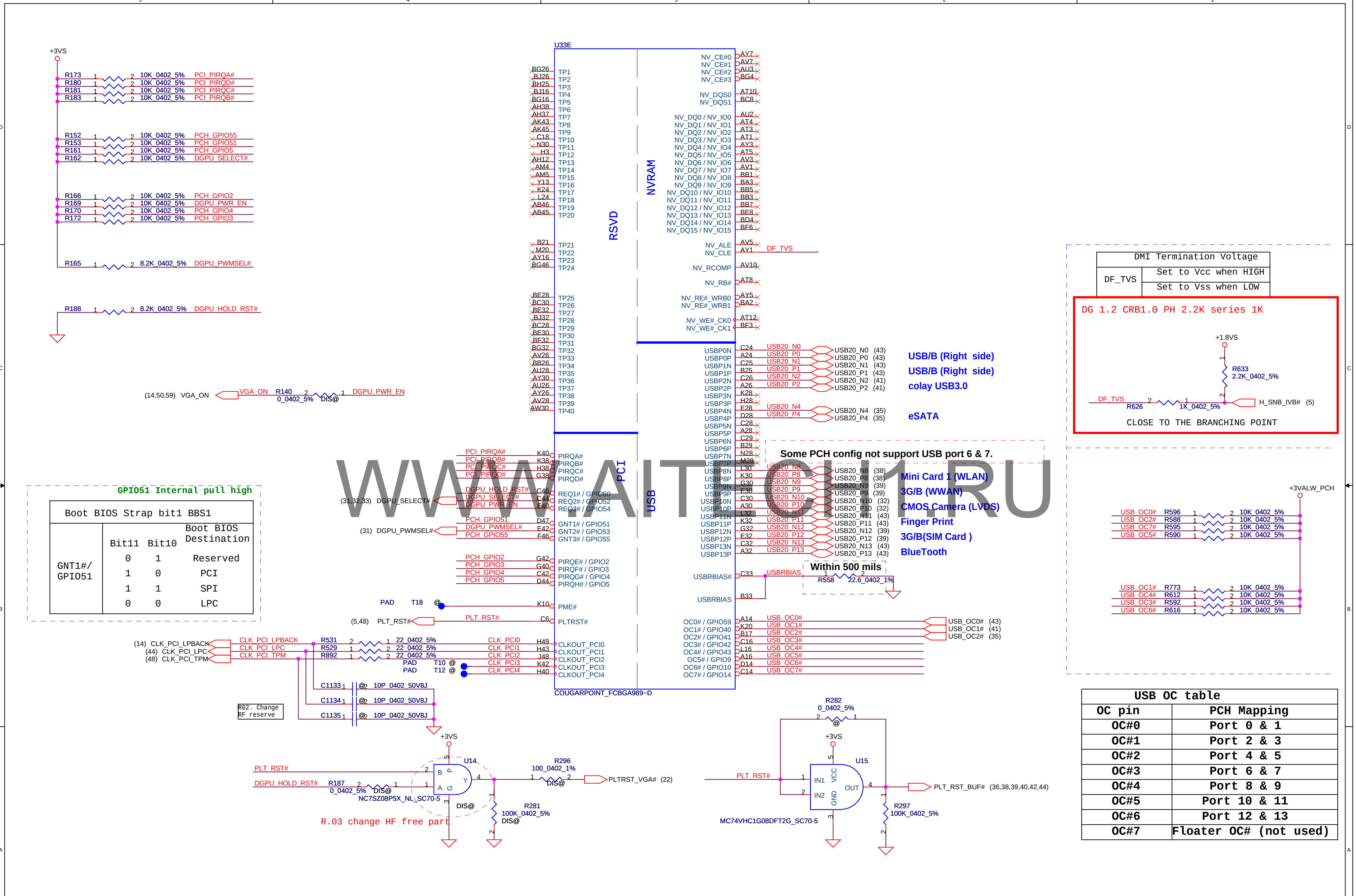

GPIO51 Internal pull high

Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Boot BIOS Destination
GNT1#/ GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC

DMI Termination Voltage	
DF_TVS	Set to Vcc when HIGH
	Set to Vss when LOW

DG 1.2 CRB1.0 PH 2.2K series 1K

USB OC table	
OC pin	PCH Mapping
OC#0	Port 0 & 1
OC#1	Port 2 & 3
OC#2	Port 4 & 5
OC#3	Port 6 & 7
OC#4	Port 8 & 9
OC#5	Port 10 & 11
OC#6	Port 12 & 13
OC#7	Floater OC# (not used)

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HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

R272 1 @ 2 1K_0402_5% PCH_GPIO28
+3VALW_PCH
R768 1 2 4.7K_0402_5%

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R661 1 2 10K_0402_5% PCH_GPIO27

+3VS
R623 1 NOPT@ 2 10K_0402_5% OPTIMUS_EN#
R639 1 OPT@ 2 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
Non-OPTIMUS	1

+3VS
R277 1 2 100K_0402_5% WWAN_OFF#
R276 1 2 10K_0402_5% PCH_GPIO0
R546 1 2 10K_0402_5% DGPU_EDIDSEL#
R191 1 2 10K_0402_5% DGPU_HPD_INT#
R641 1 2 10K_0402_5% PCH_GPIO16
R194 1 2 10K_0402_5% DGPU_PWROK
R290 1 2 10K_0402_5% PCH_GPIO22
R649 1 2 10K_0402_5% MINI1_PWR_EN#
R291 1 2 200K_0402_5% ODD_DETECT#
R619 1 2 10K_0402_5% BT_ON#
R292 1 2 10K_0402_5% MINI2_PWR_EN#
R274 1 2 10K_0402_5% WL_OFF#

+3VALW_PCH
R262 1 2 10K_0402_5% PCH_GPIO24
R620 1 2 10K_0402_5% PCH_GPIO12
R672 1 2 1K_0402_5% SMIB
R263 1 2 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

U33F

PCH_GPIO0 T7 BMBUSY# / GPIO0
(31) DGPU_EDIDSEL# DGPU_EDIDSEL# A42 TACH1 / GPIO1
(34) DGPU_HPD_INT# DGPU_HPD_INT# H36 TACH2 / GPIO6
(44) EC_SCI# EC_SCI# E38 TACH3 / GPIO7
(44) EC_SMI# EC_SMI# C10 GPIO8
PCH_GPIO12 C4 LAN_PHY_PWR_CTRL / GPIO12
(40) SMIB SMIB G2 GPIO15
(39) mSATA_DET# R195 1 2 0_0402_5% PCH_GPIO16 U2 SATA4GP / GPIO16
R.03 change short pad
DGPU_PWROK D40 TACH0 / GPIO17
PCH_GPIO22 T5 SCLOCK / GPIO22
PCH_GPIO24 E8 GPIO24 / MEM_LED
PCH_GPIO27 E16 GPIO27
PCH_GPIO28 P8 GPIO28
(38,43) BT_ON# BT_ON# K1 STP_PCI# / GPIO34
K4 GPIO35
ODD_DETECT# V8 SATA2GP / GPIO36
(39) WWAN_OFF# WWAN_OFF# M5 SATA3GP / GPIO37
OPTIMUS_EN# N2 SLOAD / GPIO38
(38) MINI1_PWR_EN# MINI1_PWR_EN# M3 SDATAOUT0 / GPIO39
(39) MINI2_PWR_EN# MINI2_PWR_EN# V13 SDATAOUT1 / GPIO48
(38) WL_OFF# WL_OFF# V3 SATA5GP / GPIO49
PCH_GPIO57 D6 GPIO57

GPIO

TACH4 / GPIO68 C40 ODD_EN#
TACH5 / GPIO69 B41 PCH_GPIO69
TACH6 / GPIO70 C41 PCH_GPIO70
TACH7 / GPIO71 A40 PCH_GPIO71

CPU/MISC

A20GATE P4 GATEA20 (44)
PECI AU16 PCH_PECI_R 1 0_0402_5% @ 2 R239 H_PECI (5,44)
RCIN# P5 EC_KBRST# EC_KBRST# (44)
PROCPWRGD AY11 H_CPUPWRGD (5)
THRMTRIP# AY10 PCH_THRMTRIP# R 1 R627 2 390_0402_5% H_THRMTRIP# H_THRMTRIP# (5)
INIT3_3V# T14

+3VS
R278 10K_0402_5%

PECI CPU-EC
CTRL-ALT-DEL
non CPU power ok
130 degree shut sown

INIT3_3V Checklist1.0 P.59
This signal has weak internal PU, can't pull low,leave NC

NC_1 AH8
NC_2 AK11
NC_3 AH10
NC_4 AK10
NC_5 P37

TS_VSS1~4 PD to GND

NCTF

VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BE1
VSS_NCTF_14 BE49

VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

PAD T61 @ PAD T58
PAD T46 @ PAD T39
PAD T44 @ PAD T59
PAD T41 @ PAD T40
PAD T52 @ PAD T60
PAD T51 @ PAD T45
PAD T64 @ PAD T43
PAD T37 @ PAD T42
PAD T55 @ PAD T50
PAD T34 @ PAD T49
PAD T56 @ PAD T65
PAD T35 @ PAD T38
PAD T57 @ PAD T63
PAD T36 @ PAD T32
PAD T54
PAD T33
PAD T53
PAD T31

COUGARPOINT_FCBGA989-D

R.03 Change
+3VSDGPU
R709 10K_0402_5% DIS@
R1130 100K_0402_5% DIS@
Q64 2N7002E_SOT23-3 DIS@
Q63 2N7002E_SOT23-3 DIS@
C1137 1U_0402_6.3V6K DIS@
DGPU_PWROK

+3VS
ODD_EN# R771 1 2 10K_0402_5%
EC_KBRST# R279 1 2 10K_0402_5%

+3VS
R554 10K_0402_5% @ PCH_GPIO69
R548 10K_0402_5% @ PCH_GPIO70
R553 10K_0402_5%
R549 10K_0402_5%

+3VS
R550 10K_0402_5% @ PCH_GPIO71
R551 10K_0402_5%

Project ID	GPIO69	GPIO70
* P4VC0	0	0
x	0	1
x	1	0
x	1	1

	GPIO71 PCH_GPIO71
*VRAM 800 MHz	0
VRAM 900 MHz	1

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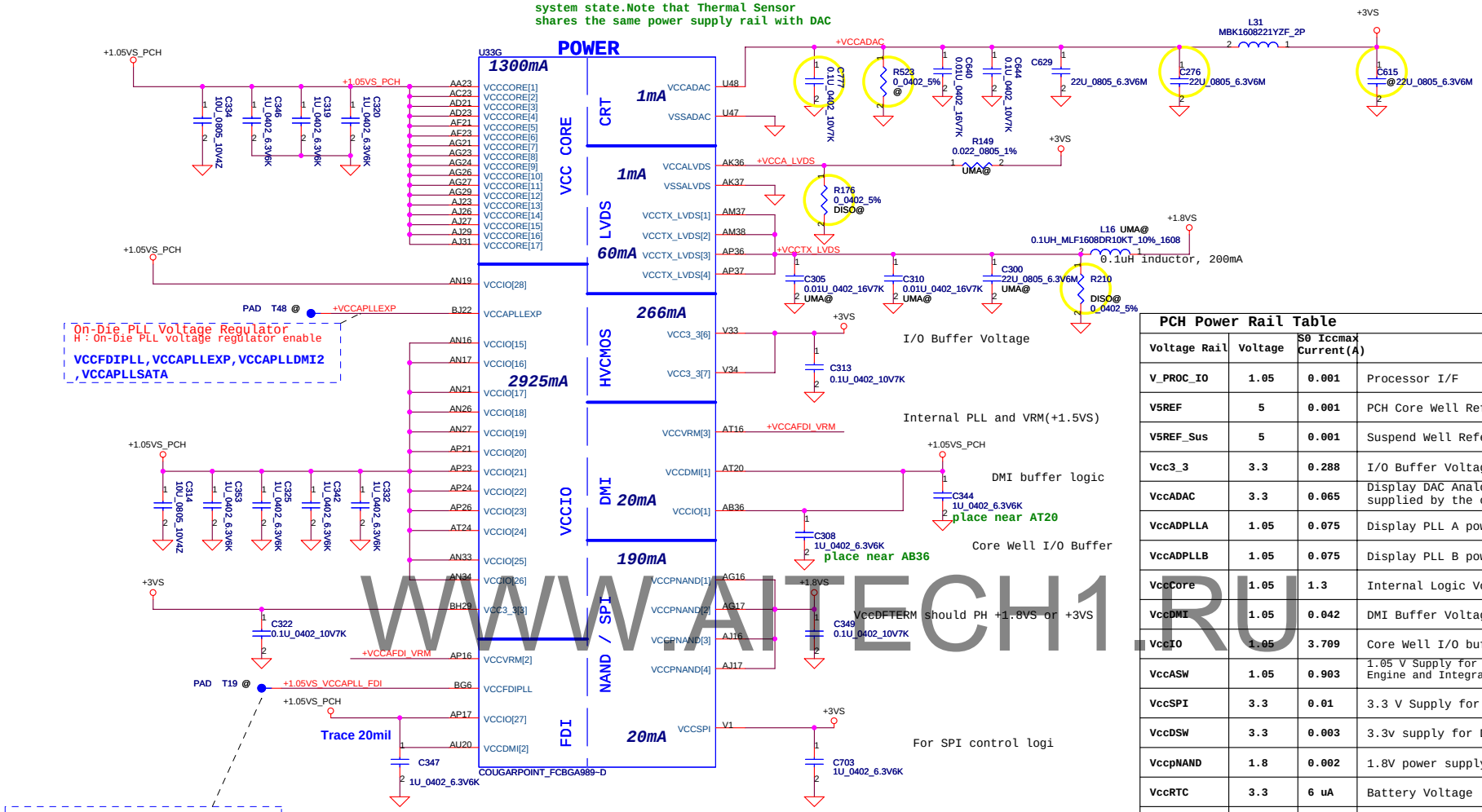

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.288	I/O Buffer Voltage
VccADAC	3.3	0.065	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.075	Display PLL A power
VccADPLLB	1.05	0.075	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	3.709	Core Well I/O buffers
VccASW	1.05	0.903	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.002	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.119	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.167	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.075	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.04	Analog power supply for LVDS (Mobile Only)

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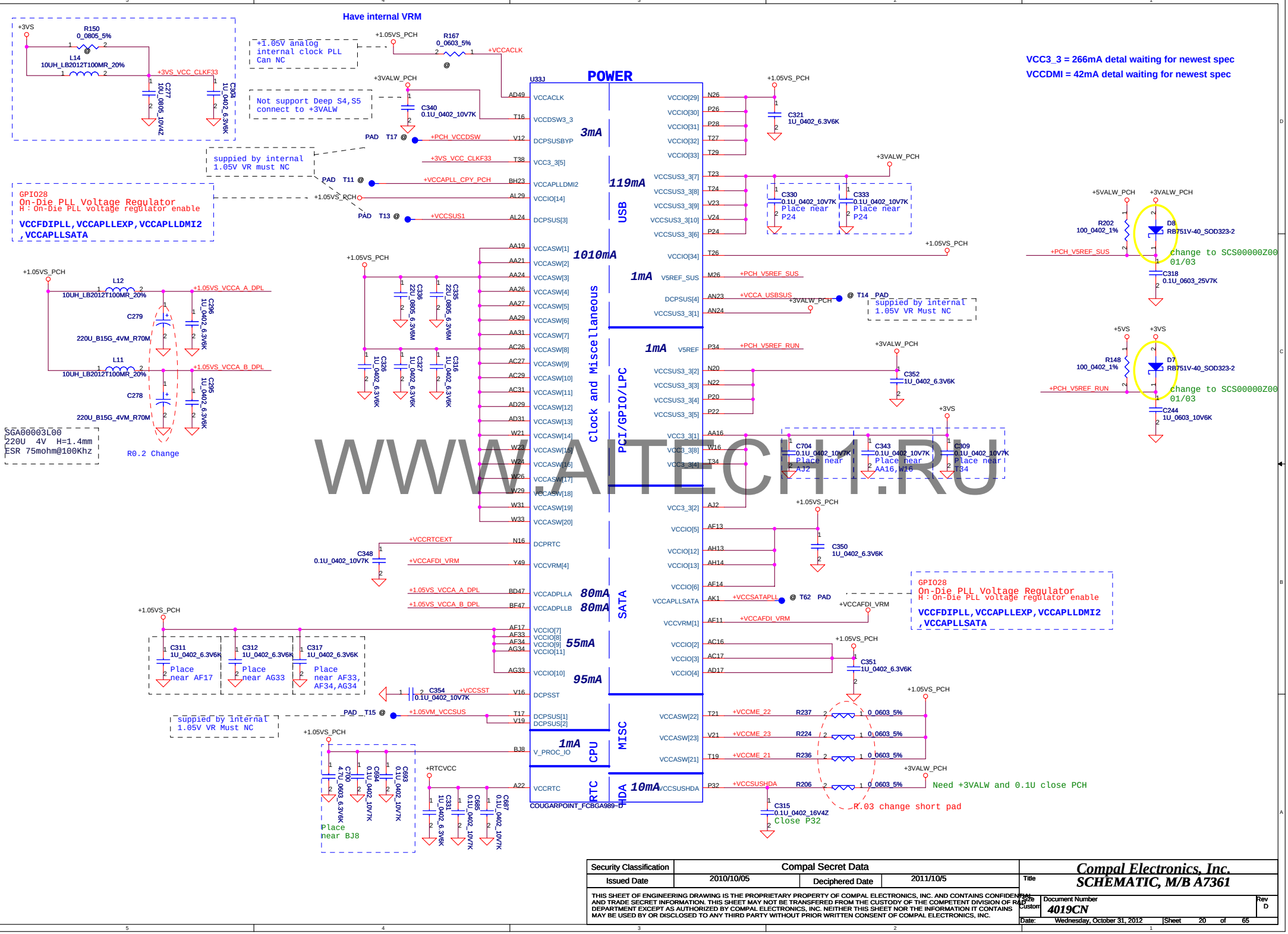

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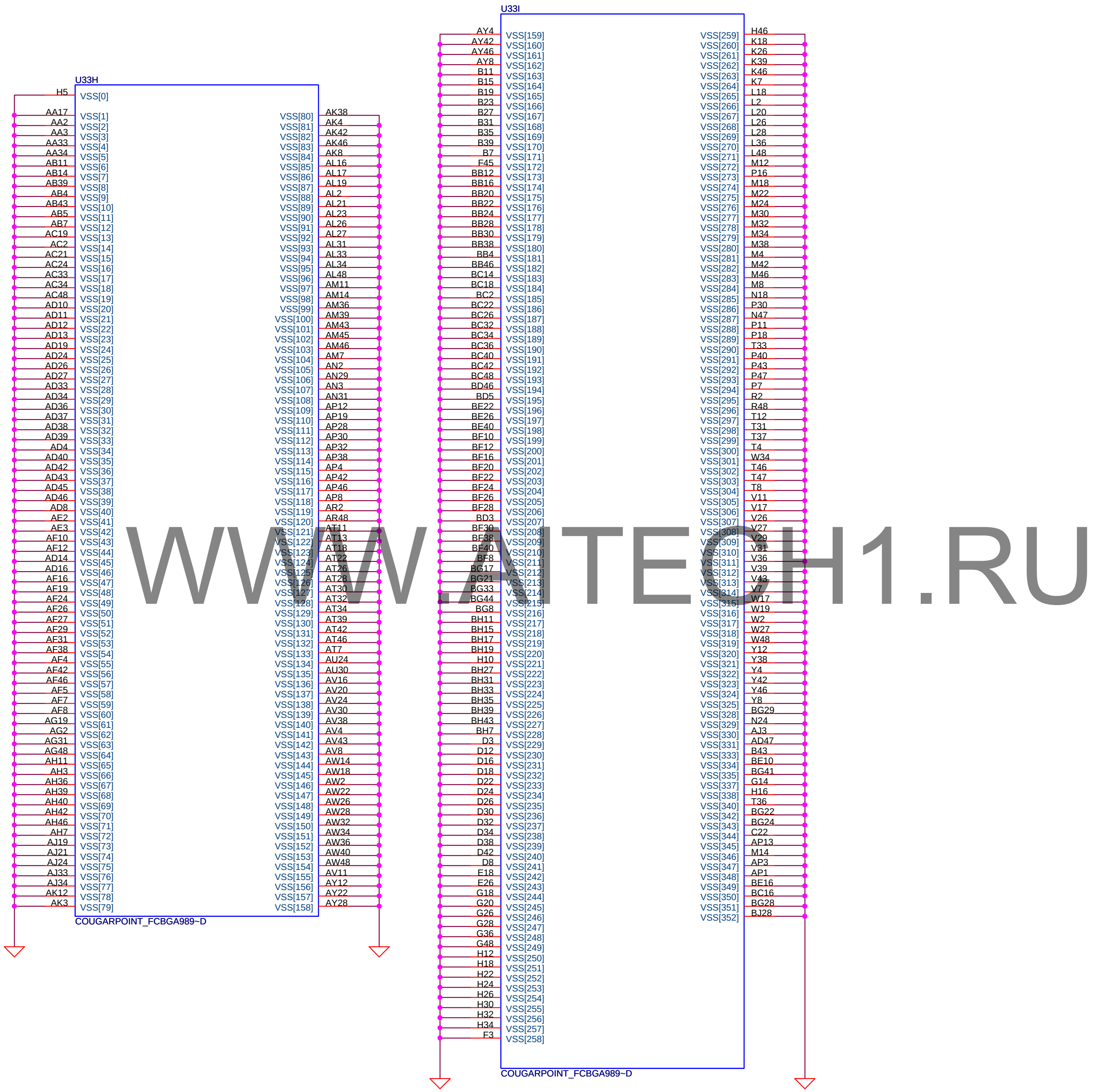

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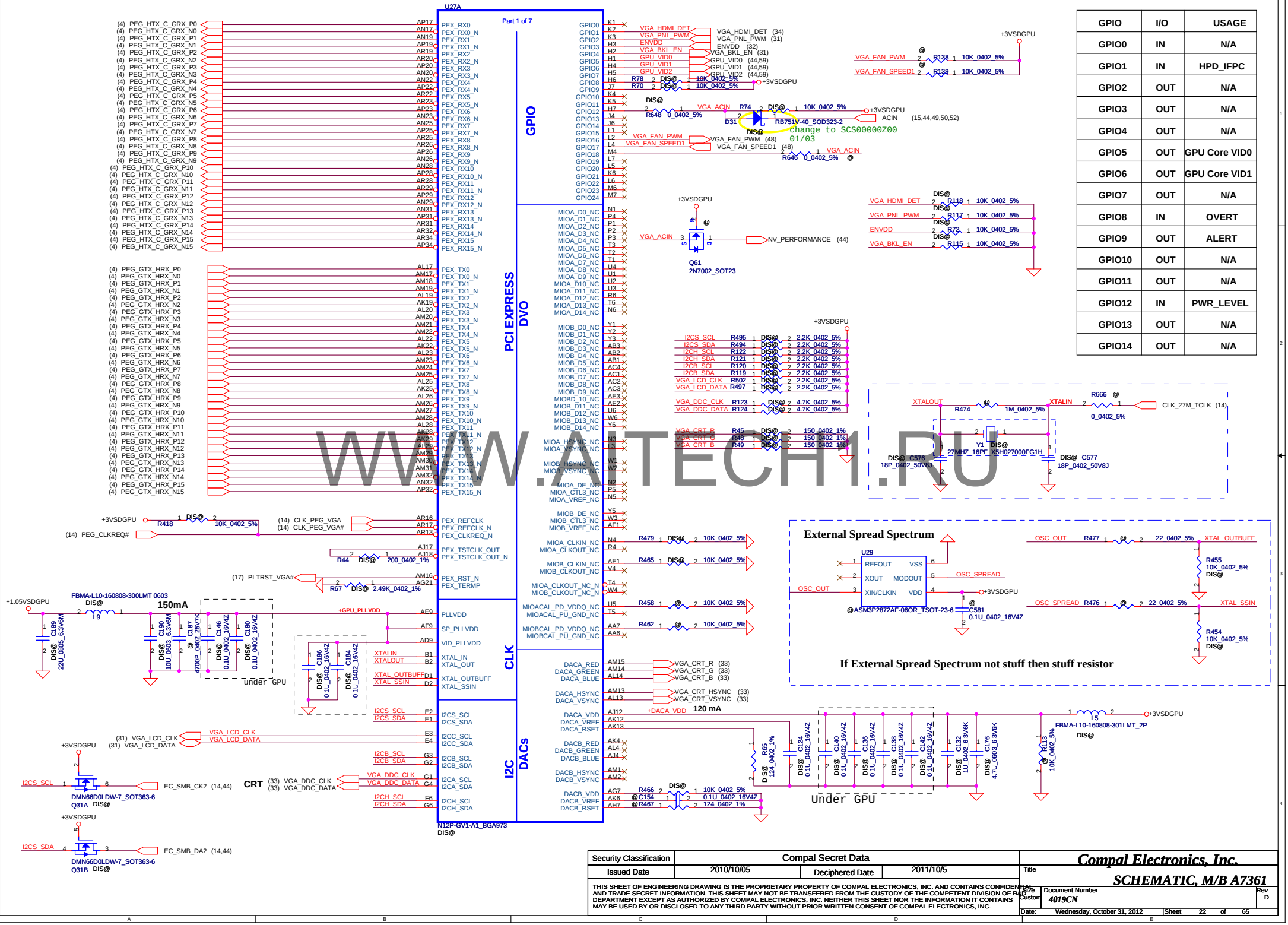

GPIO	I/O	USAGE
GPIO0	IN	N/A
GPIO1	IN	HPD_IFPC
GPIO2	OUT	N/A
GPIO3	OUT	N/A
GPIO4	OUT	N/A
GPIO5	OUT	GPU Core VID0
GPIO6	OUT	GPU Core VID1
GPIO7	OUT	N/A
GPIO8	IN	OVERT
GPIO9	OUT	ALERT
GPIO10	OUT	N/A
GPIO11	OUT	N/A
GPIO12	IN	PWR_LEVEL
GPIO13	OUT	N/A
GPIO14	OUT	N/A

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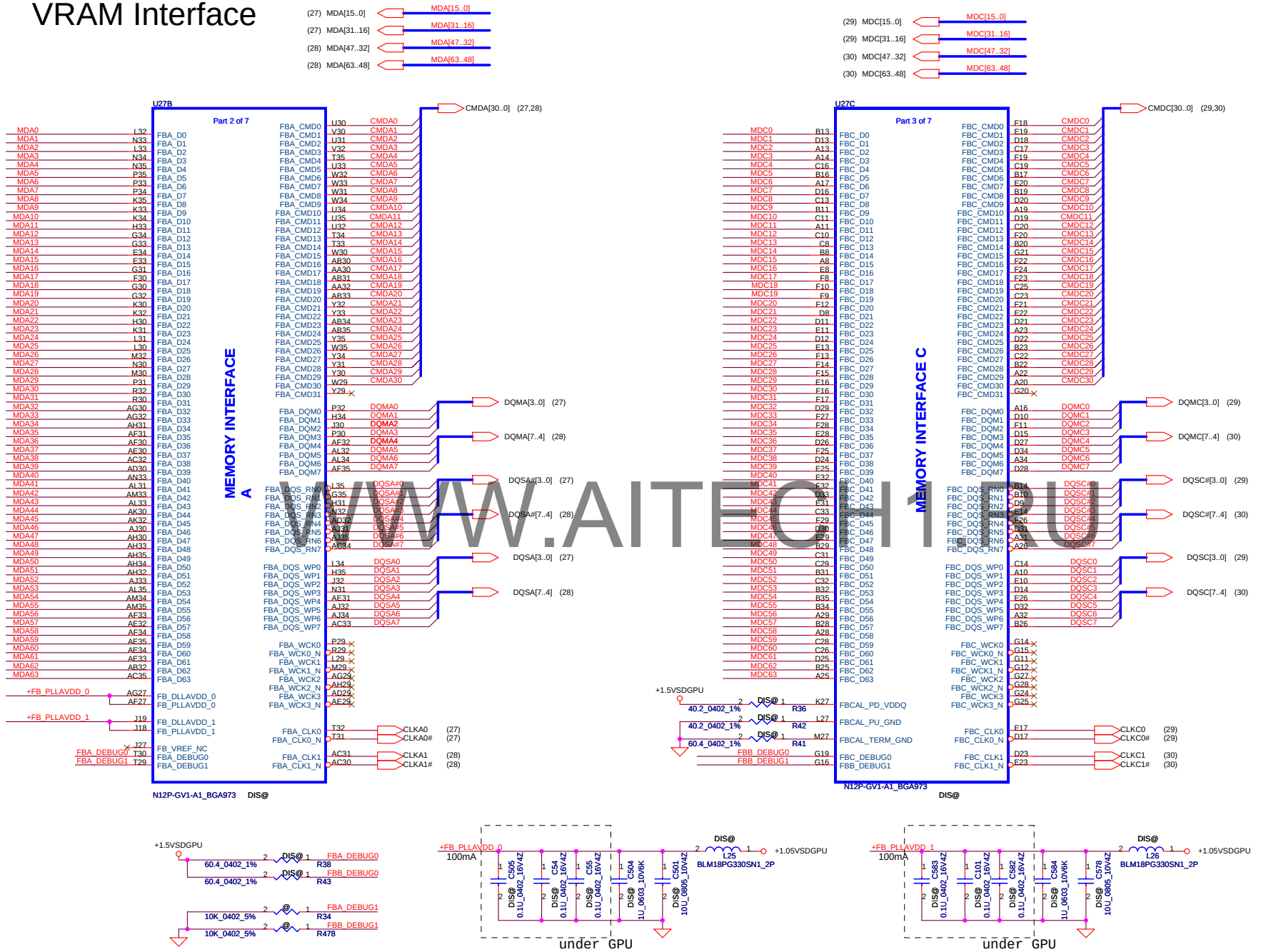
VRAM Interface



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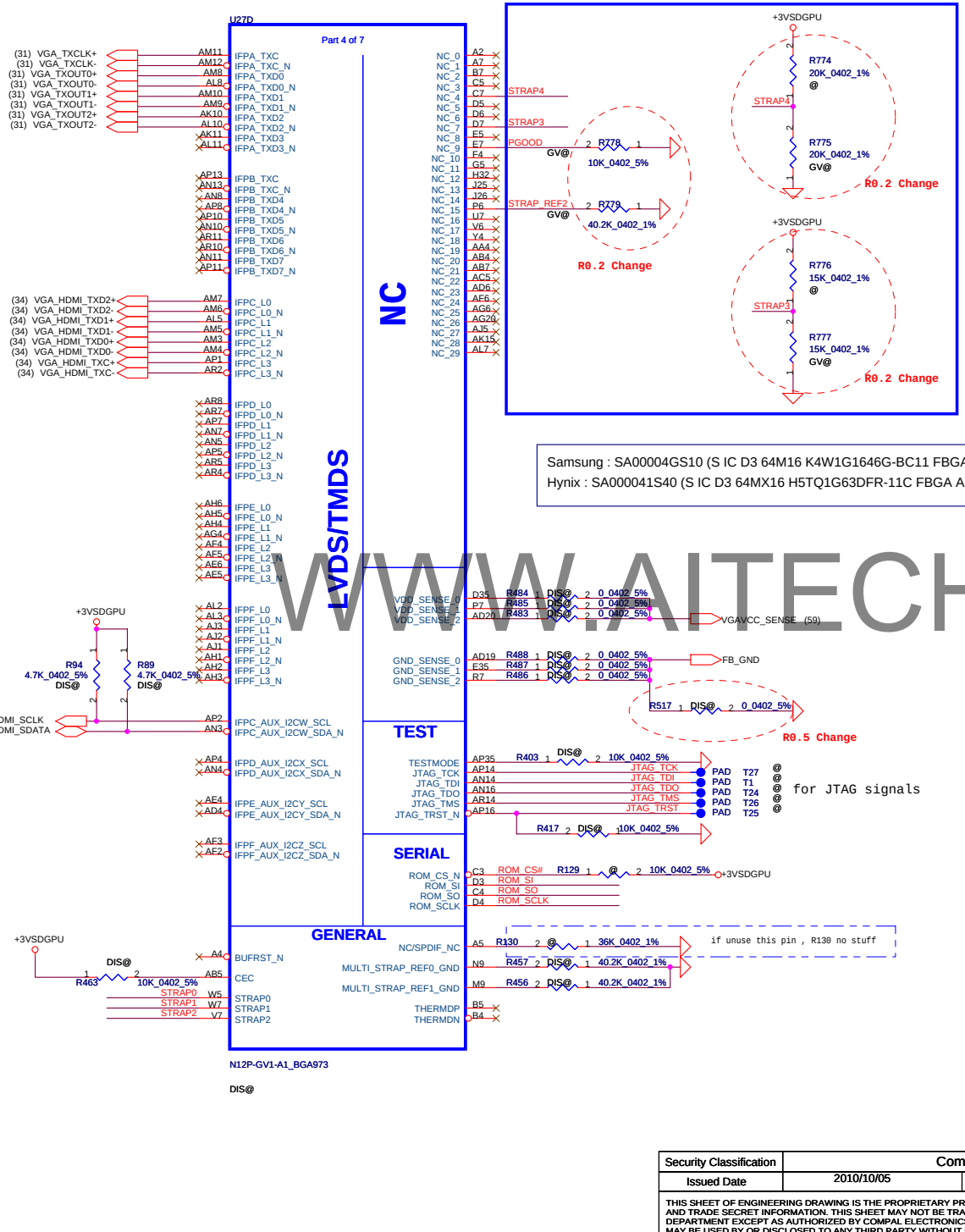
For GB2-128 & GB2b-128 colayout....



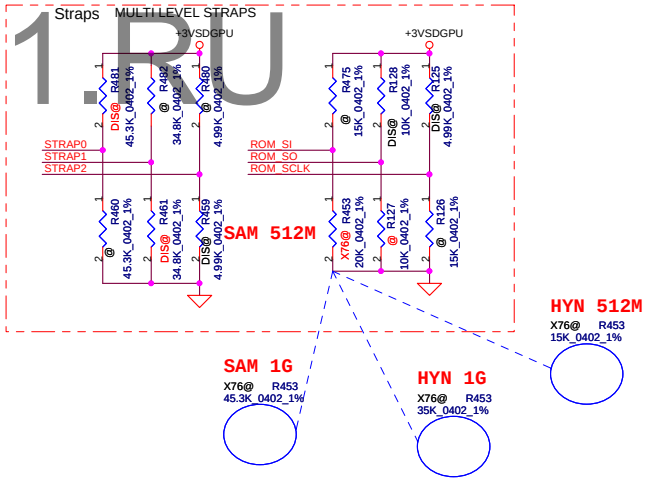
Samsung : SA00004GS10 (S IC D3 64M16 K4W1G1646G-BC11 FBGA ABO!)
Hynix : SA000041S40 (S IC D3 64MX16 H5TQ1G63DFR-11C FBGA ABO!)

For N12P-GS strap table
(strap 3 and strap4 left NC)

Frenq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K

Default
For N12P-GV strap table

Frenq.	N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK	strap3	strap4
900 MHz	64MX16 Hynix SA000041S40	H 45K	L 35K	L 5K	L 15K	H 10K	H 5K	L 15K	L 20K
900 MHz	64MX16 Samsung SA00004GS10	H 45K	L 35K	L 5K	L 20K	H 10K	H 5K	L 15K	L 20K
900 MHz	128MX16 Hynix SA00003YO20	H 45K	L 35K	L 5K	L 35K	H 10K	H 5K	L 15K	L 20K
900 MHz	128MX16 Samsung SA000047Q20	H 45K	L 35K	L 5K	L 45K	H 10K	H 5K	L 15K	L 20K



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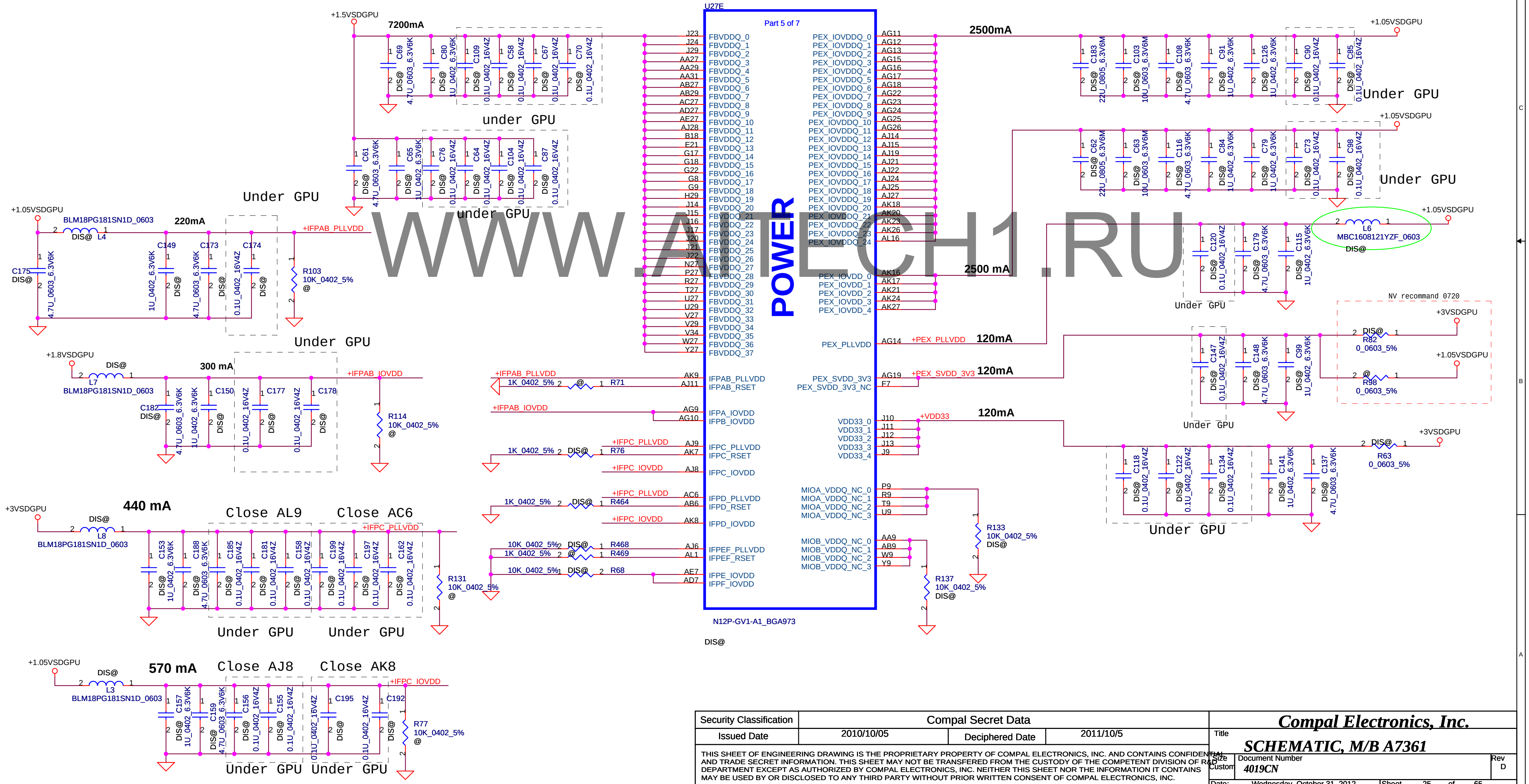

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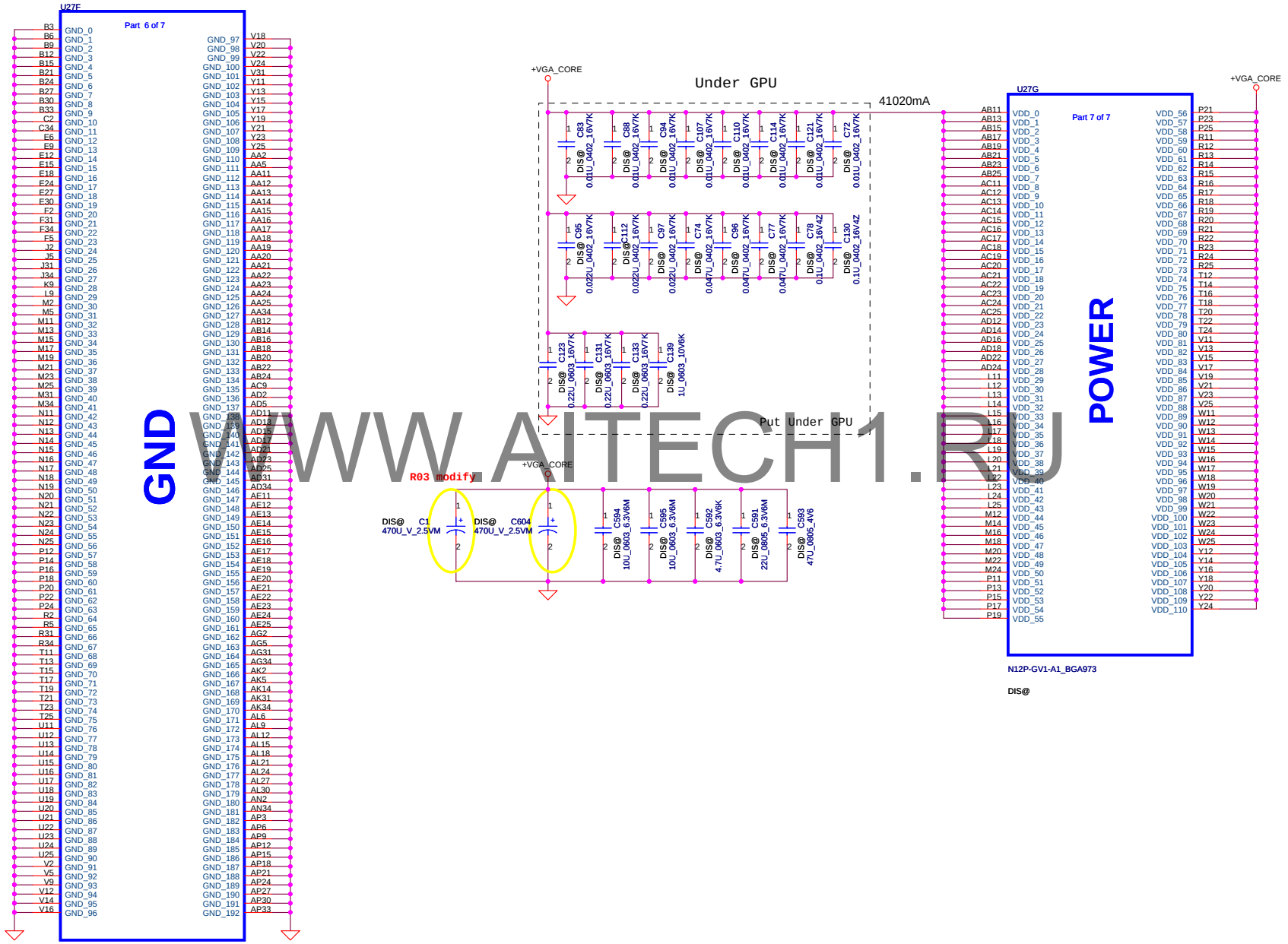

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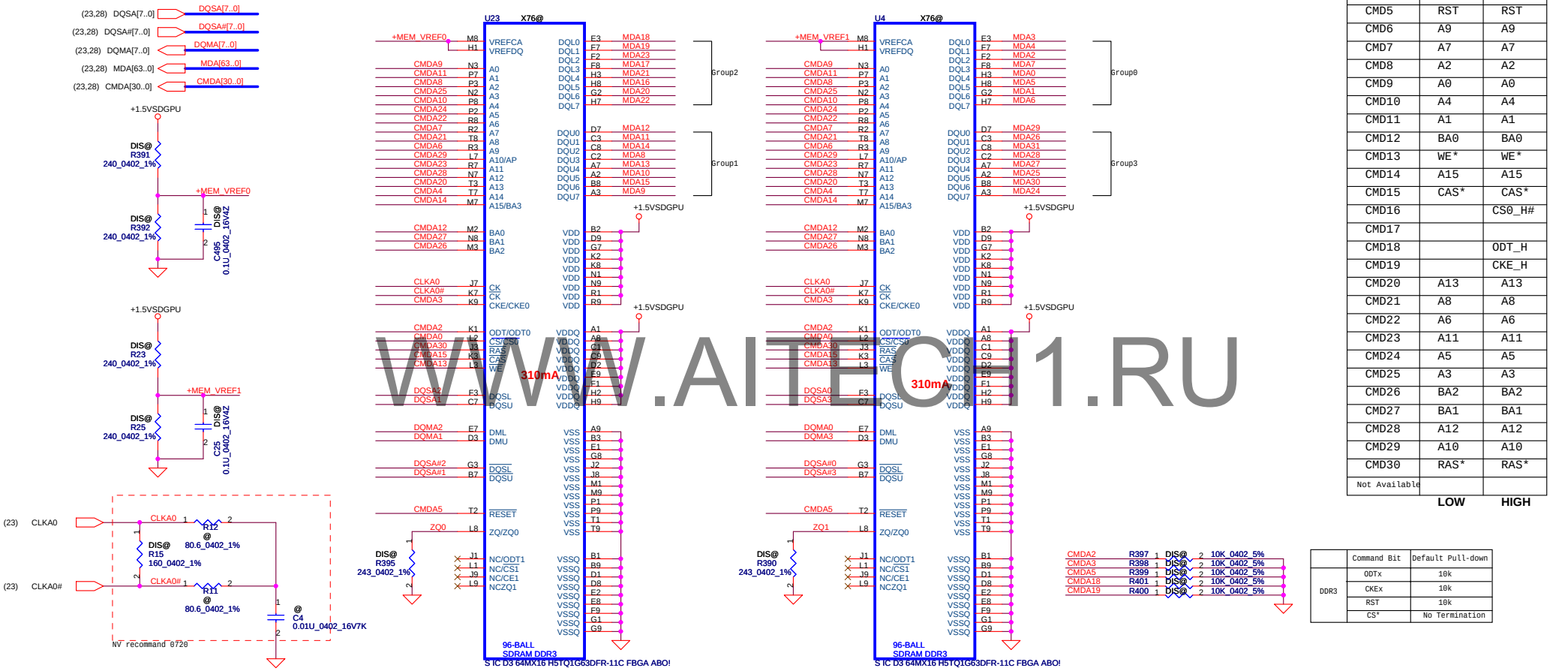
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Samsung : SA00004GS10 (S IC D3 64M16 K4W1G1646G-BC11 FBGA ABO!)
Hynix : SA000041S40 (S IC D3 64MX16 H5TQ1G63DFR-11C FBGA ABO!)

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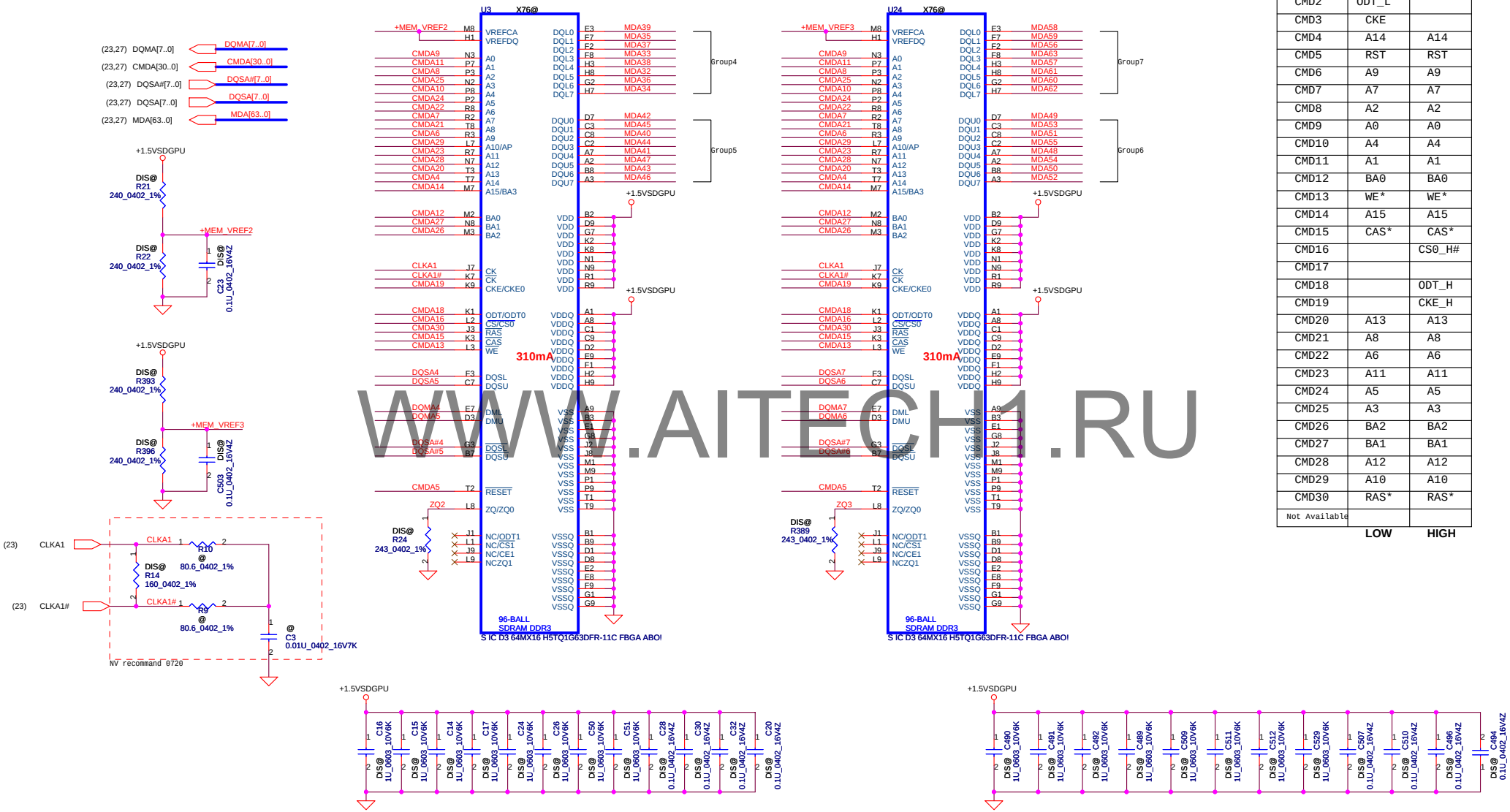
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
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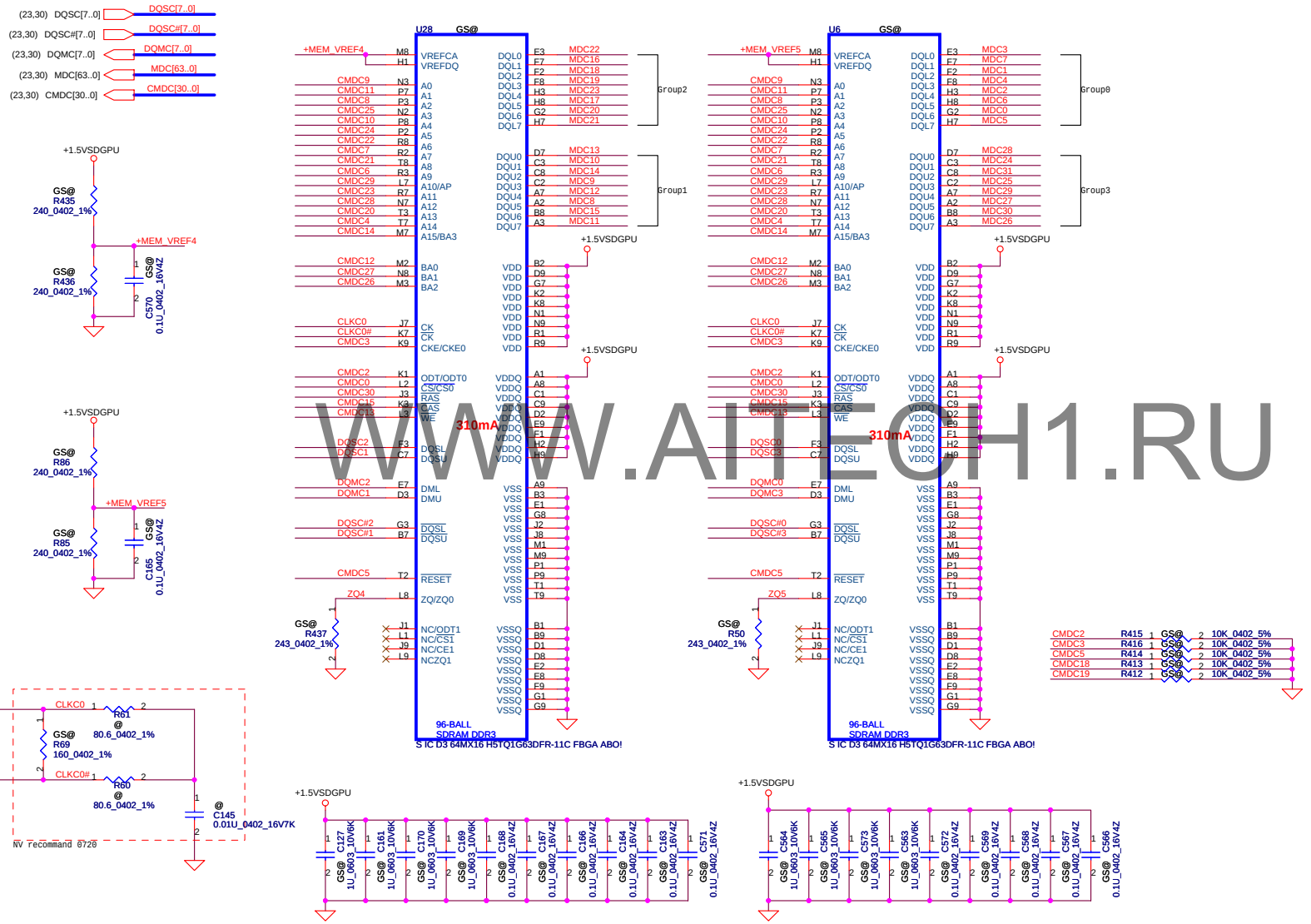
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Security Classification	Compal Secret Data		
Issued Date	2010/10/05	Deciphered Date	2011/10/5

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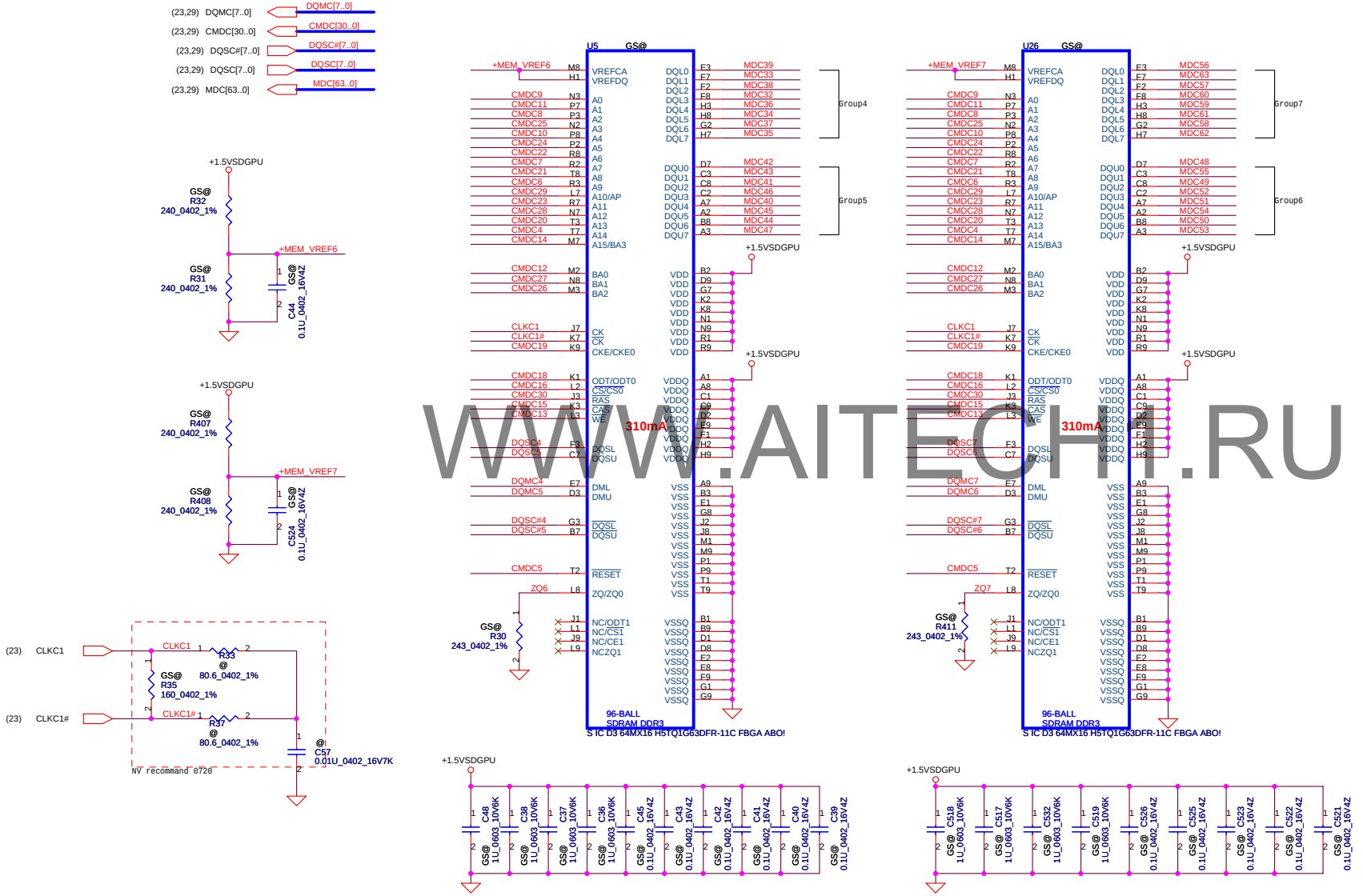
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2010/10/05	Deciphered Date	2011/10/5

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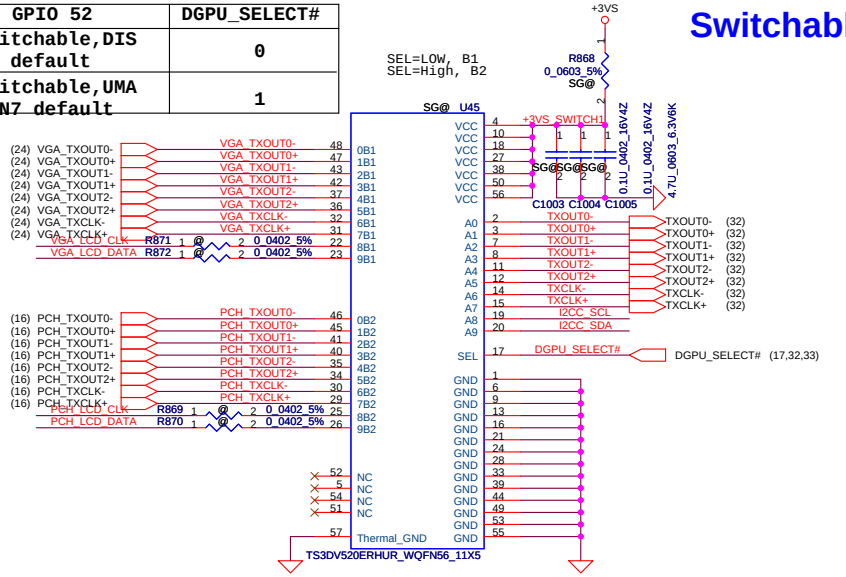
GPIO 52	DGPU_SELECT#
Switchable,DIS XP default	0
Switchable,UMA WIN7 default	1

Switchable LVDS

SEL=LOW, B1
SEL=High, B2



UMA Only

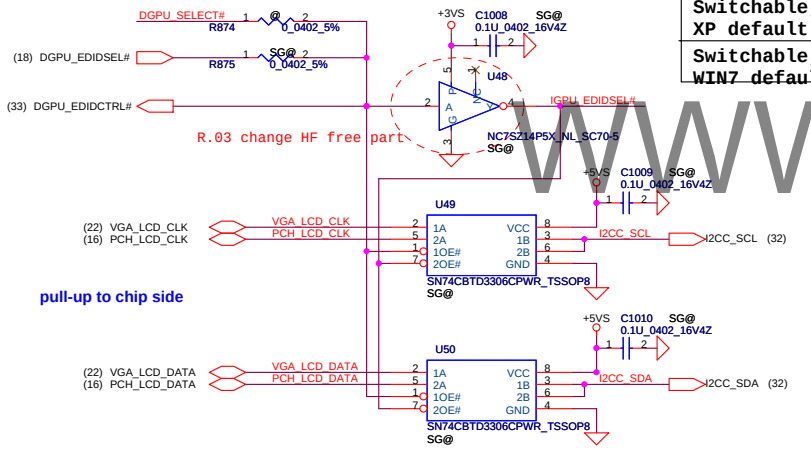
TXOUT0+	0_0402_5%	UMA@	R471	PCH_TXOUT0+	
TXOUT0-	0_0402_5%	UMA@	R473	PCH_TXOUT0-	
TXOUT1+	0_0402_5%	UMA@	R441	PCH_TXOUT1+	
TXOUT1-	0_0402_5%	UMA@	R452	PCH_TXOUT1-	
TXOUT2+	0_0402_5%	UMA@	R434	PCH_TXOUT2+	
TXOUT2-	0_0402_5%	UMA@	R439	PCH_TXOUT2-	
TXCLK+	0_0402_5%	UMA@	R432	PCH_TXCLK+	
TXCLK-	0_0402_5%	UMA@	R430	PCH_TXCLK-	
I2CC_SCL	0_0402_5%	UMA@	R504	PCH_LCD_CLK	
I2CC_SDA	0_0402_5%	UMA@	R499	PCH_LCD_DATA	
ENBKL	0_0402_5%	UMA@	R532	IGPU_BKLT_EN	
INVTPWM	0_0402_5%	UMA@	R582	DPST_PWM	

Discrete ONLY

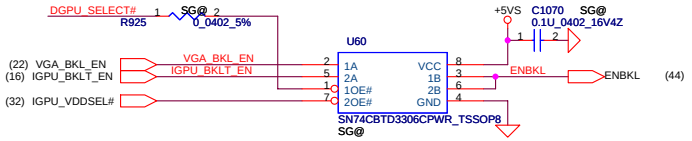
TXOUT0+	0_0402_5%	DISO@	R470	VGA_TXOUT0+	
TXOUT0-	0_0402_5%	DISO@	R472	VGA_TXOUT0-	
TXOUT1+	0_0402_5%	DISO@	R440	VGA_TXOUT1+	
TXOUT1-	0_0402_5%	DISO@	R451	VGA_TXOUT1-	
TXOUT2+	0_0402_5%	DISO@	R433	VGA_TXOUT2+	
TXOUT2-	0_0402_5%	DISO@	R438	VGA_TXOUT2-	
TXCLK+	0_0402_5%	DISO@	R431	VGA_TXCLK+	
TXCLK-	0_0402_5%	DISO@	R429	VGA_TXCLK-	
I2CC_SCL	0_0402_5%	DISO@	R503	VGA_LCD_CLK	
I2CC_SDA	0_0402_5%	DISO@	R498	VGA_LCD_DATA	
ENBKL	0_0402_5%	DISO@	R536	VGA_BKL_EN	
INVTPWM	0_0402_5%	DISO@	R609	VGA_PNL_PWM	

Switchable I2C

GPIO 01	DGPU_EDIDSEL#
Switchable,DIS XP default	0
Switchable,UMA WIN7 default	1

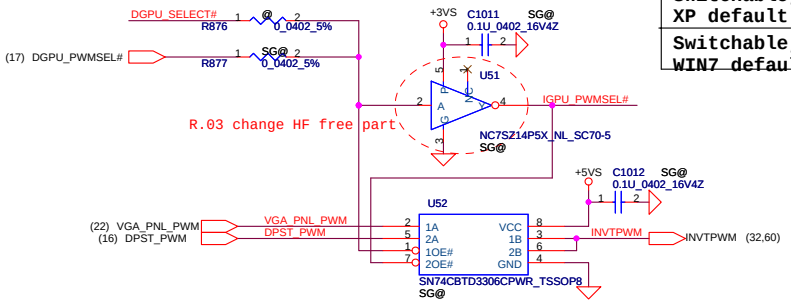


Switchable BKL_EN



Switchable PWM

GPIO 53	DGPU_PWMSEL#
Switchable,DIS XP default	0
Switchable,UMA WIN7 default	1



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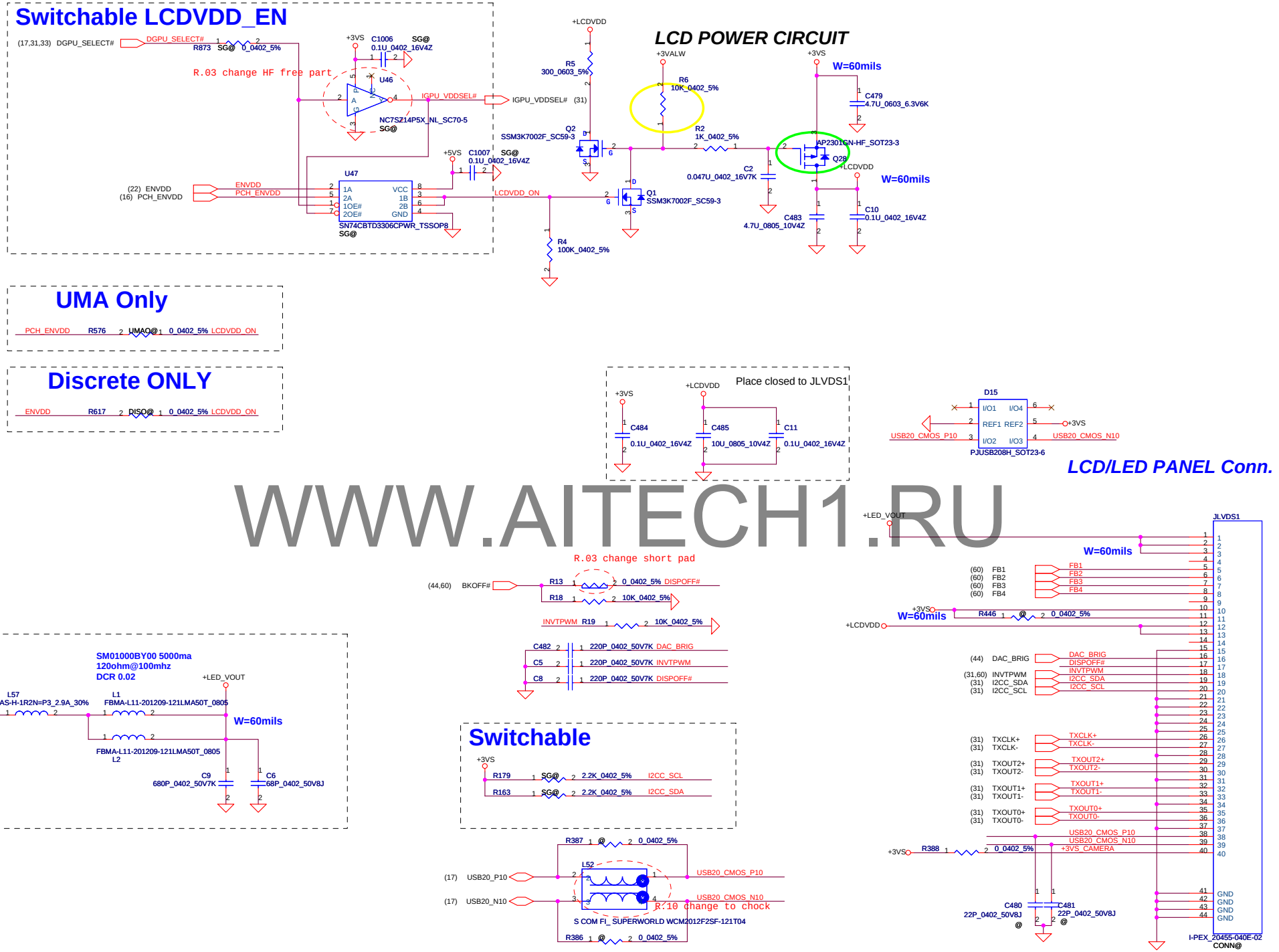

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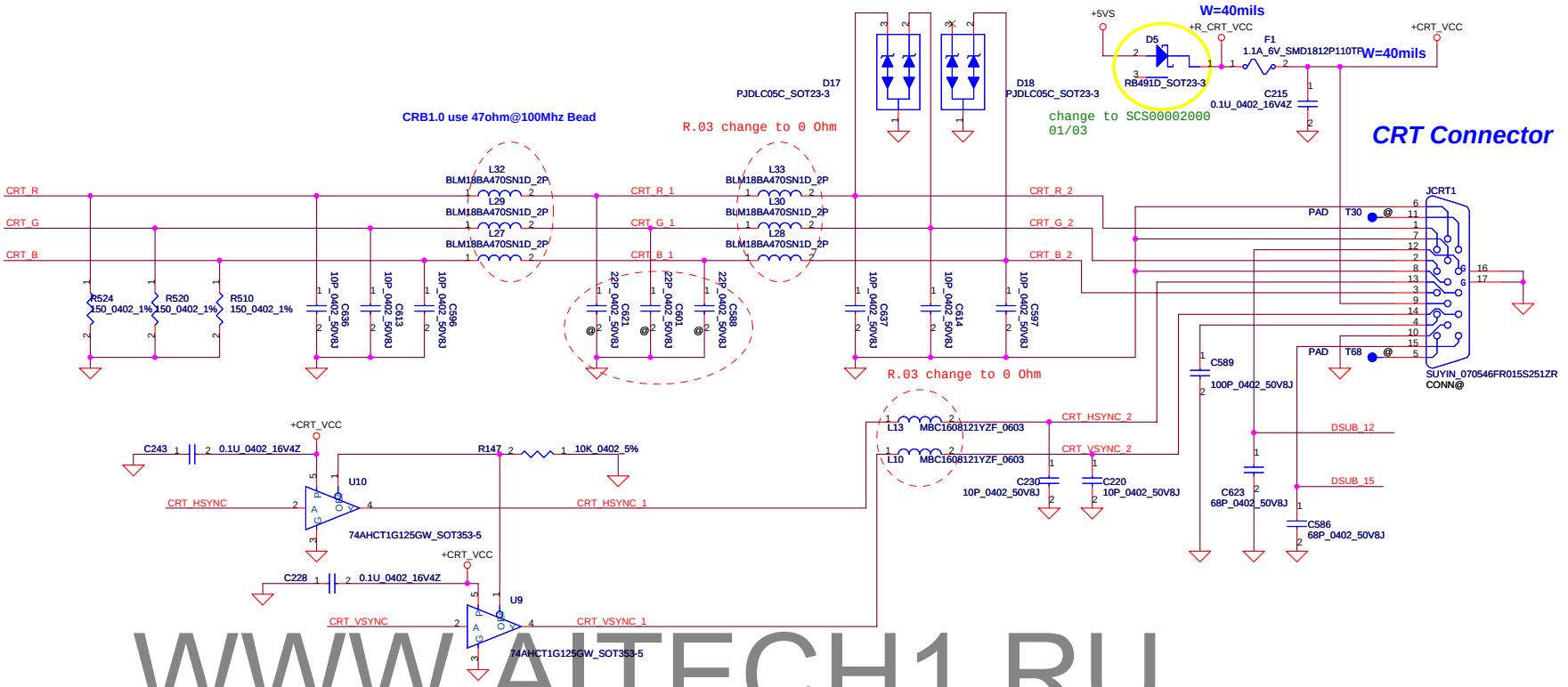
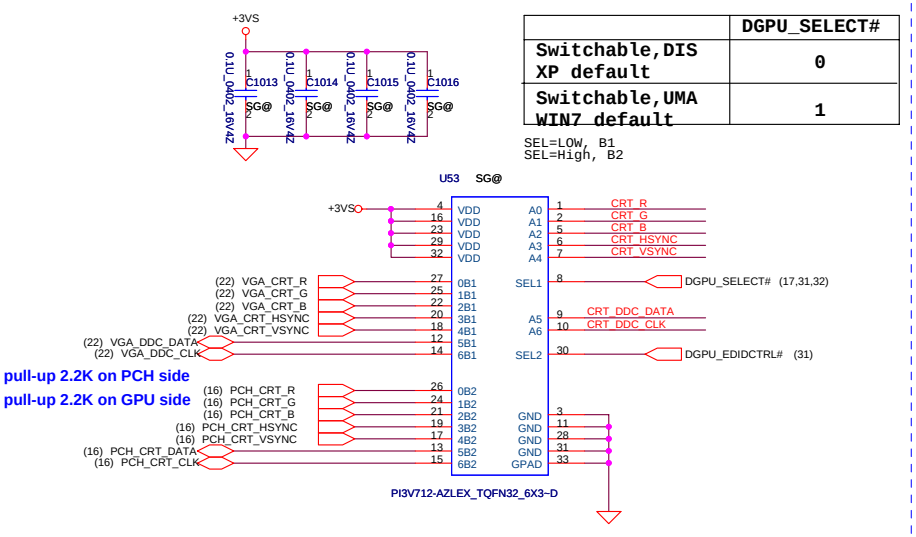


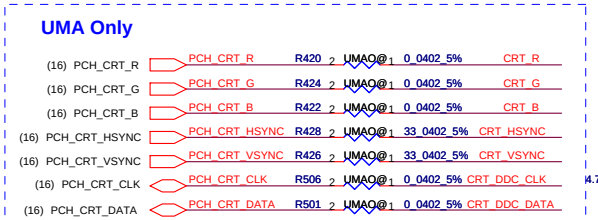
Switchable



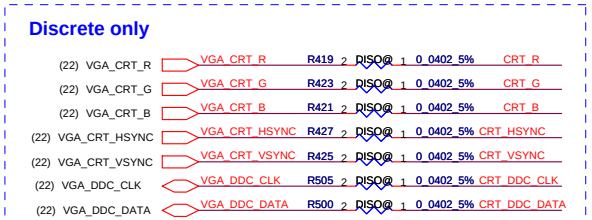
	DGPU_SELECT#
Switchable,DIS XP default	0
Switchable,UMA WIN7 default	1

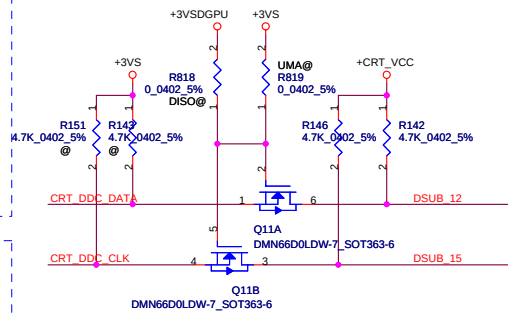
SEL=LOW, B1
SEL=High, B2

UMA Only



Discrete only





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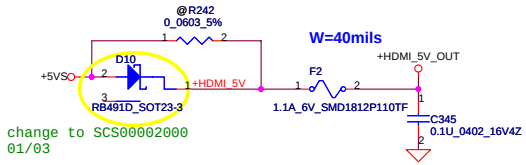
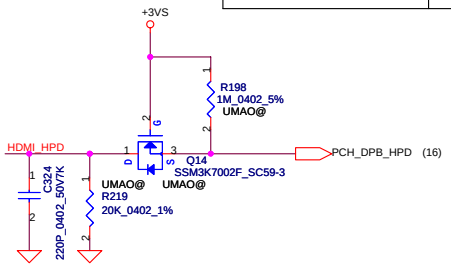
SM070001310 400ma 90ohm@100mhz DCR 0.3

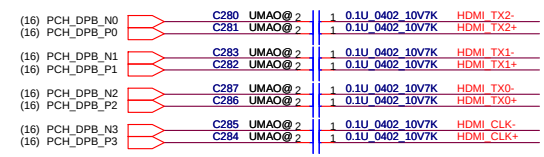


UMA HPD

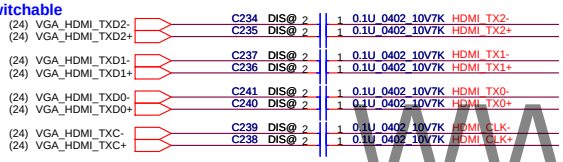
	R219
HDMI passive level shift	20K ohm
HDMI with level shift	100K ohm



UMA only

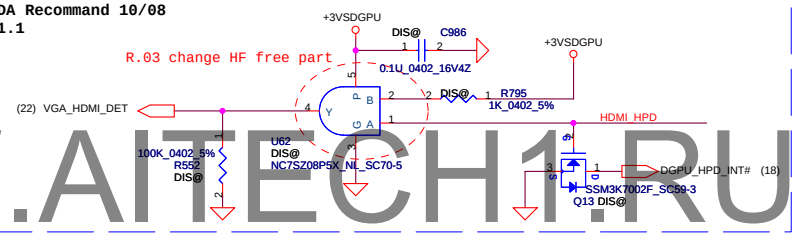


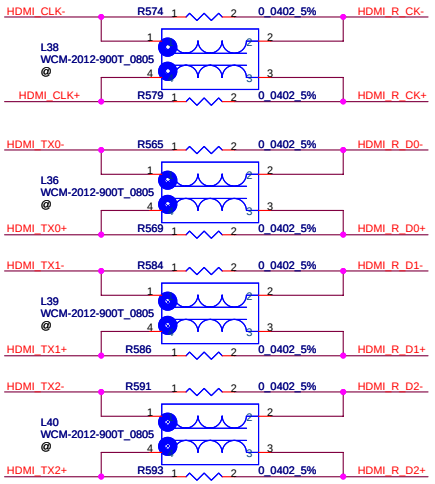
DIS only / Switchable



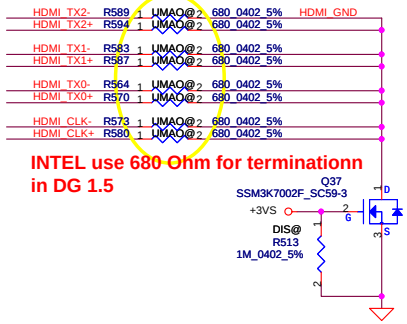
NVIDA Recommand 10/08
OPT1.1

R.03 change HF free part

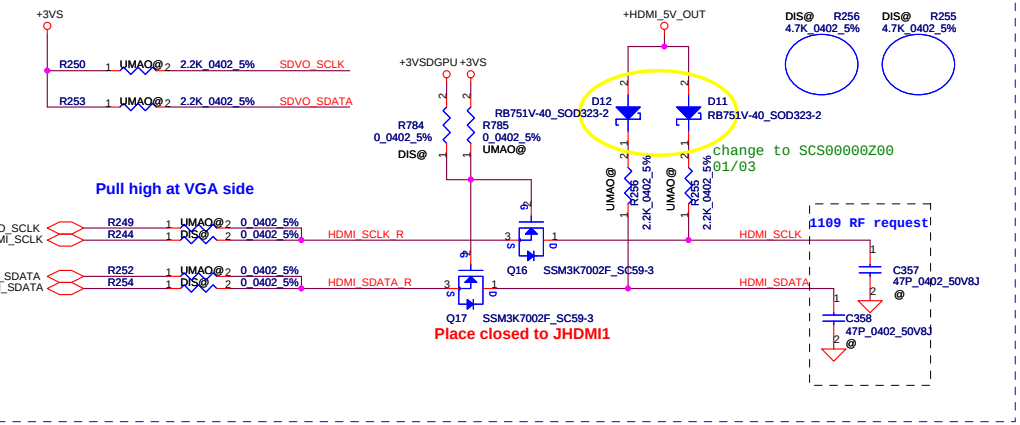




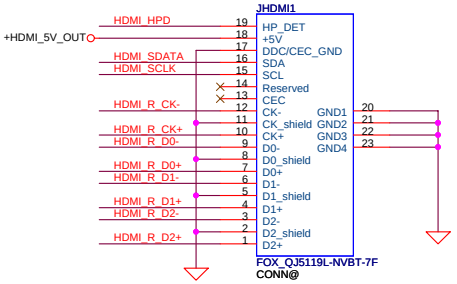
R03 modify



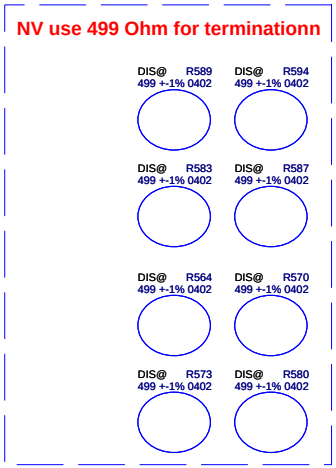
INTEL use 680 Ohm for terminationn in DG 1.5



HDMI connector



NV use 499 Ohm for terminationn



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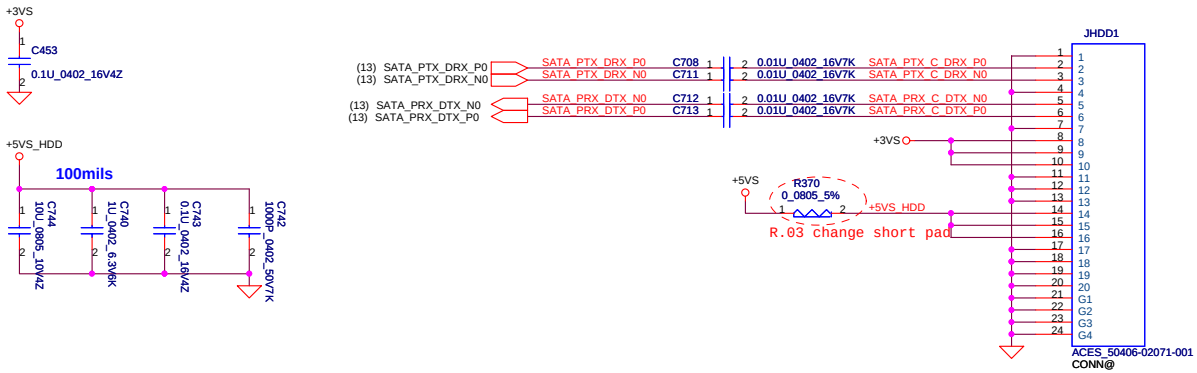
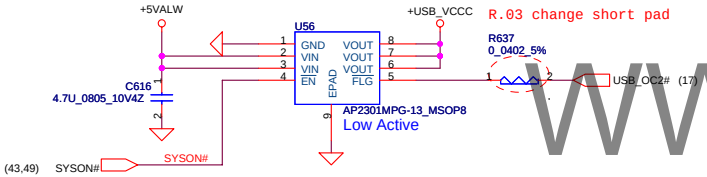
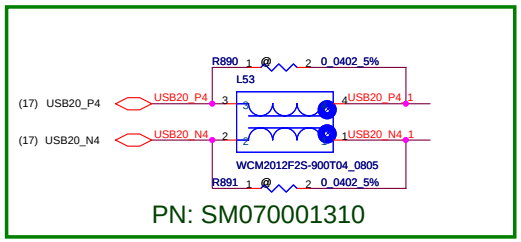
SATA HDD1 Conn.

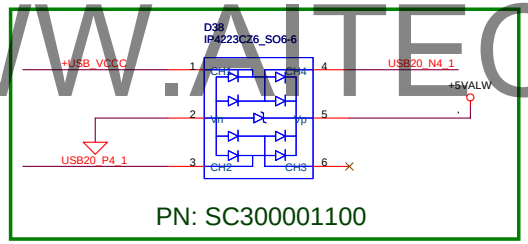


eSATA and USB Conn.



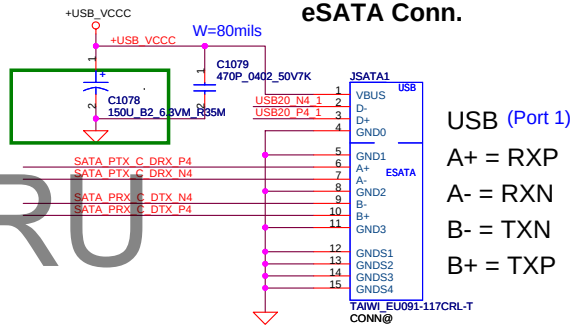


PN: SM070001310

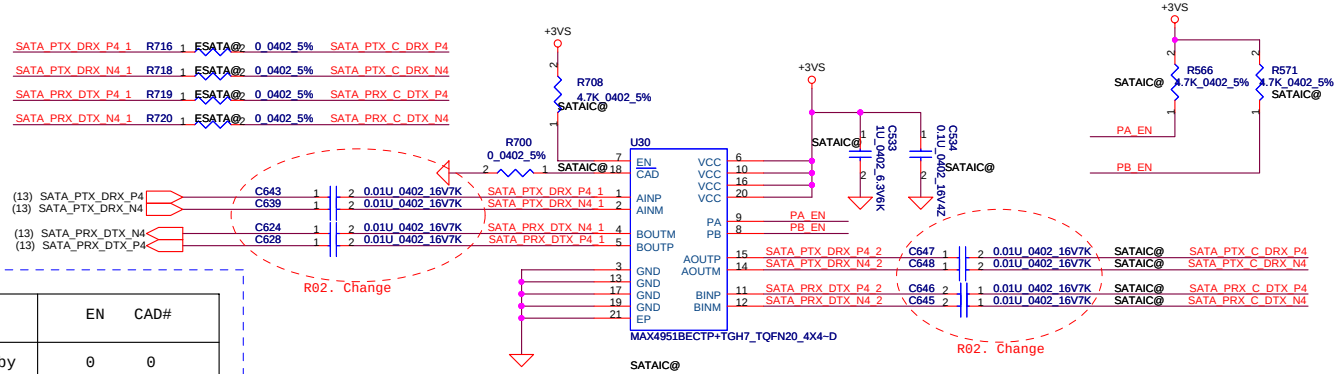


PN: SC300001100

eSATA Conn.



USB (Port 1)
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP



STATUS	EN	CAD#
Low-Power Standby	0	0
Low-Power Standby	0	1
Active	1	0
Low-Power Standby	1	1

PA、PB Internal pull down

Channel A	Channel B	EN	PA	PB
Standby	Standby	0	X	X
Standard SATA	Standard SATA	1	0	0
Preemphasis	Standard SATA	1	1	0
Standard SATA	Preemphasis	1	0	1
Preemphasis	Preemphasis	1	1	1

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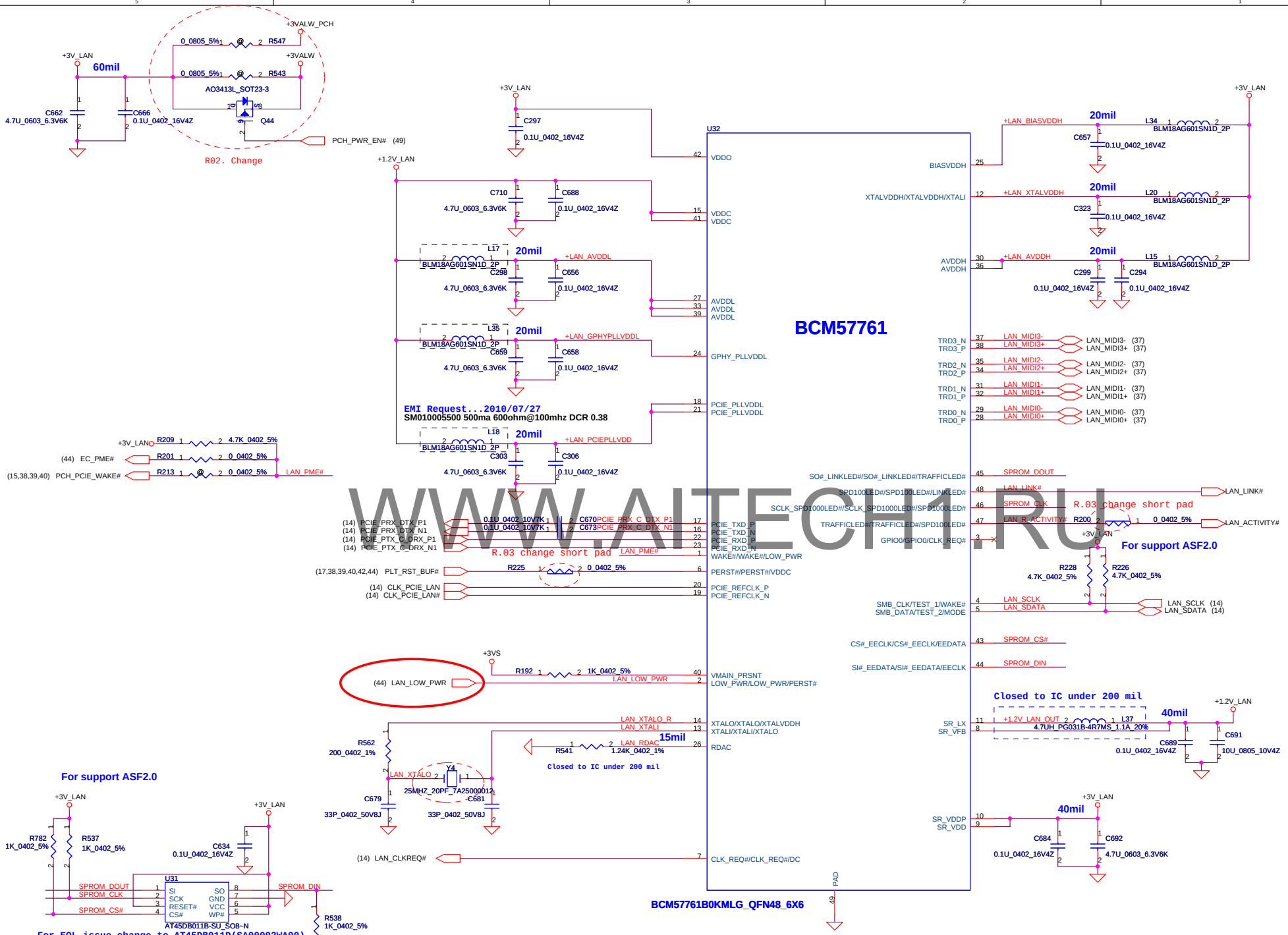

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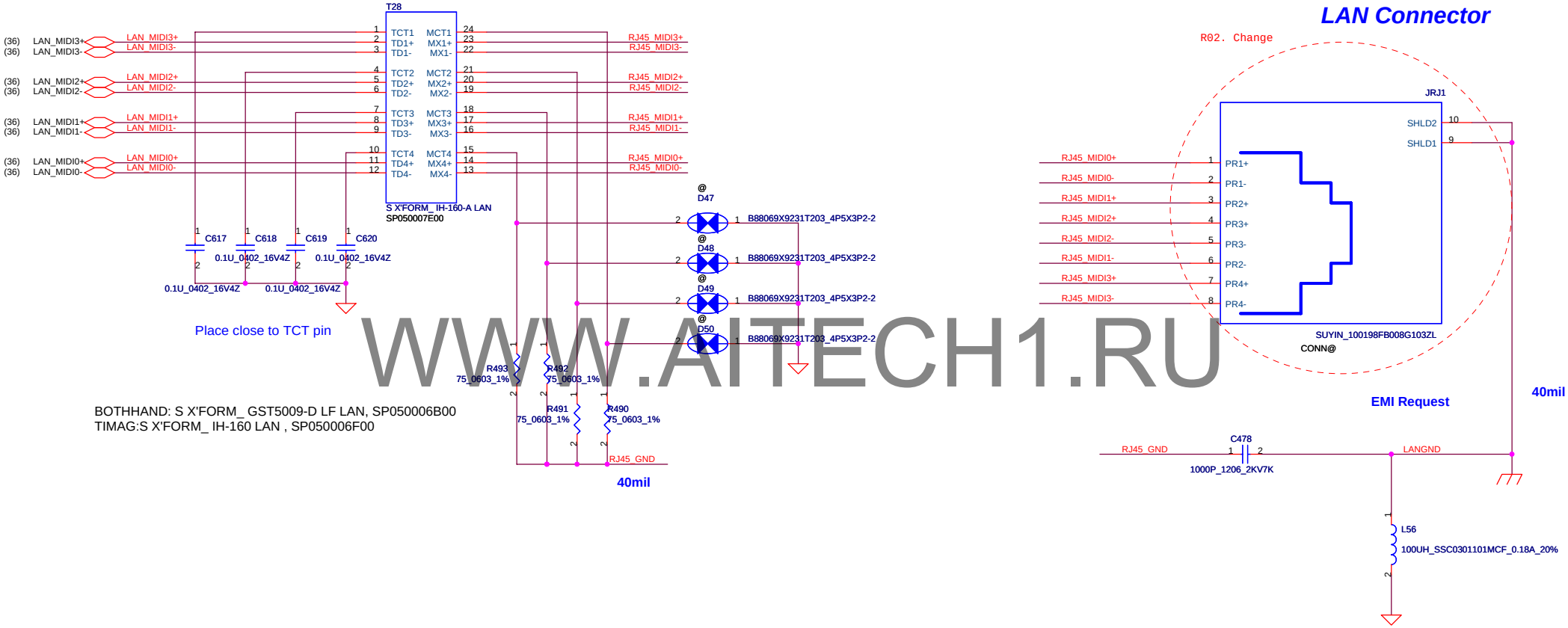

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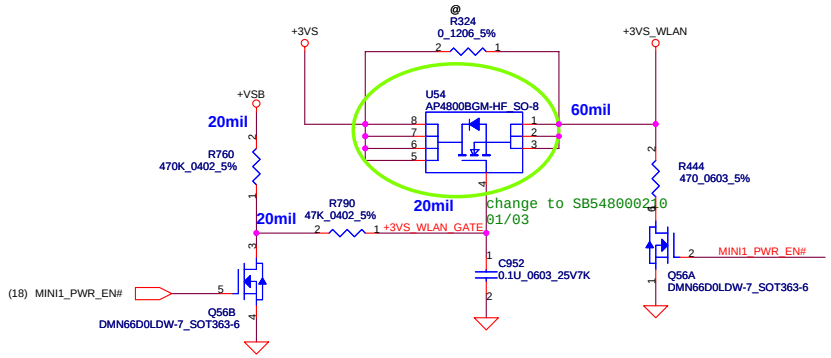
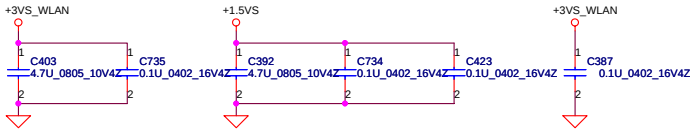
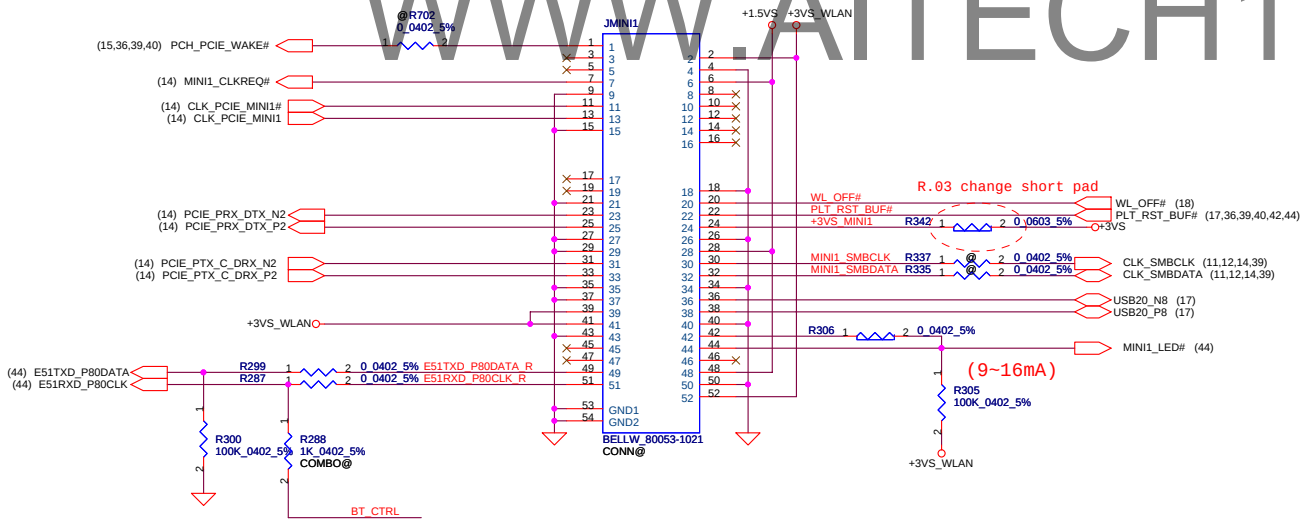
For Wireless LAN



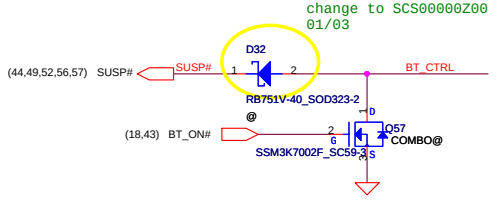
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)





WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H



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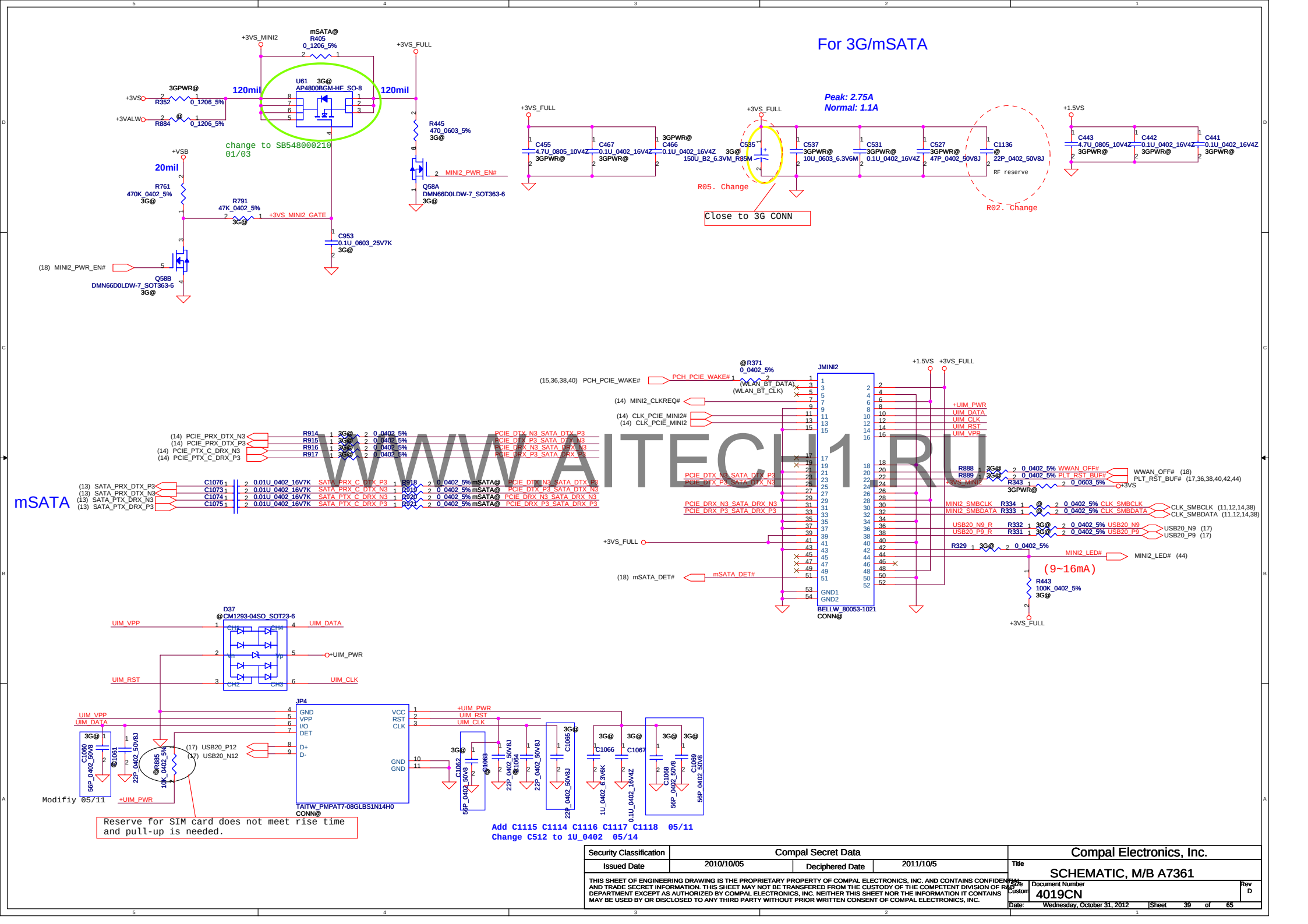

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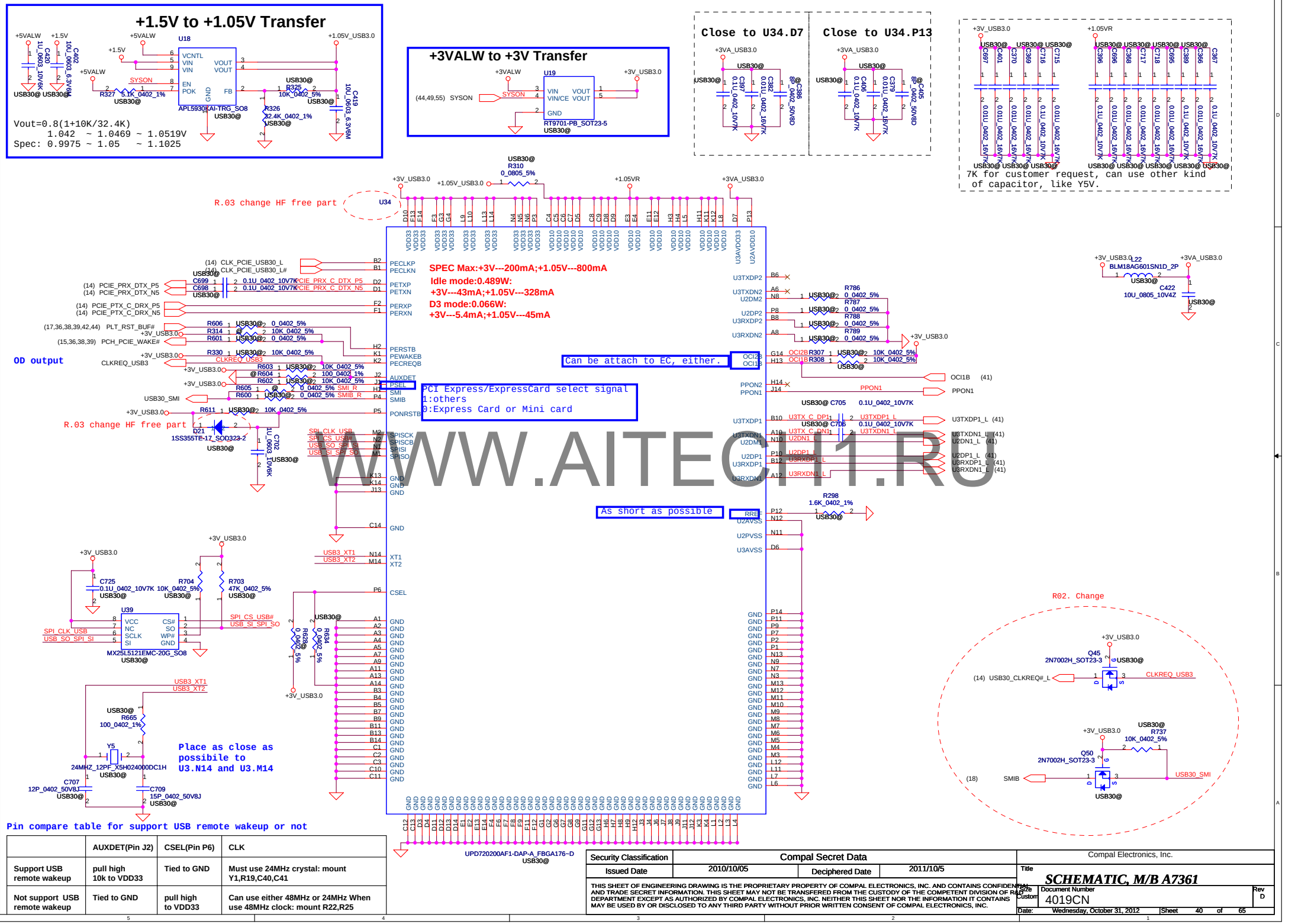

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

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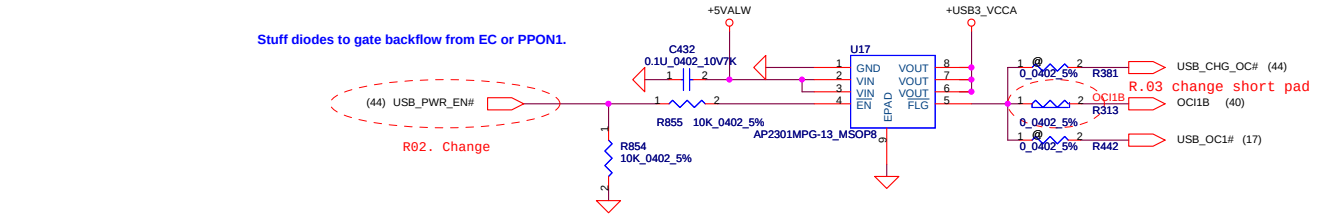
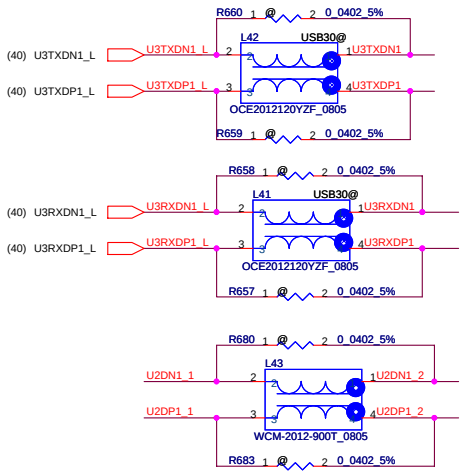
W=60mils

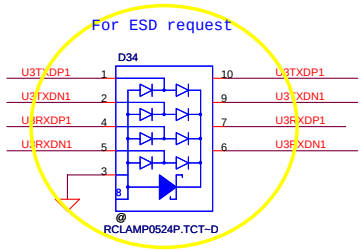
Stuff diodes to gate backflow from EC or PPON1.



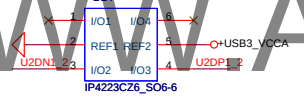
For EMI request

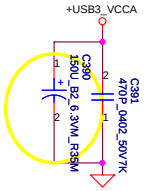


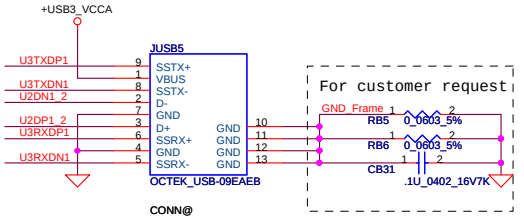
For ESD request

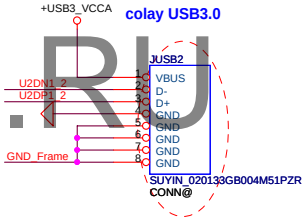


For USB2.0 ESD request

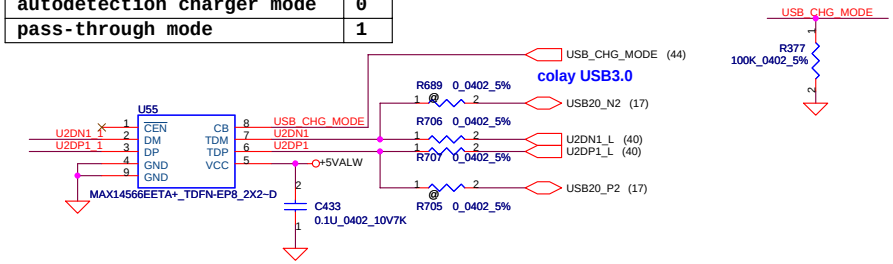








	CB
autodetection charger mode	0
pass-through mode	1



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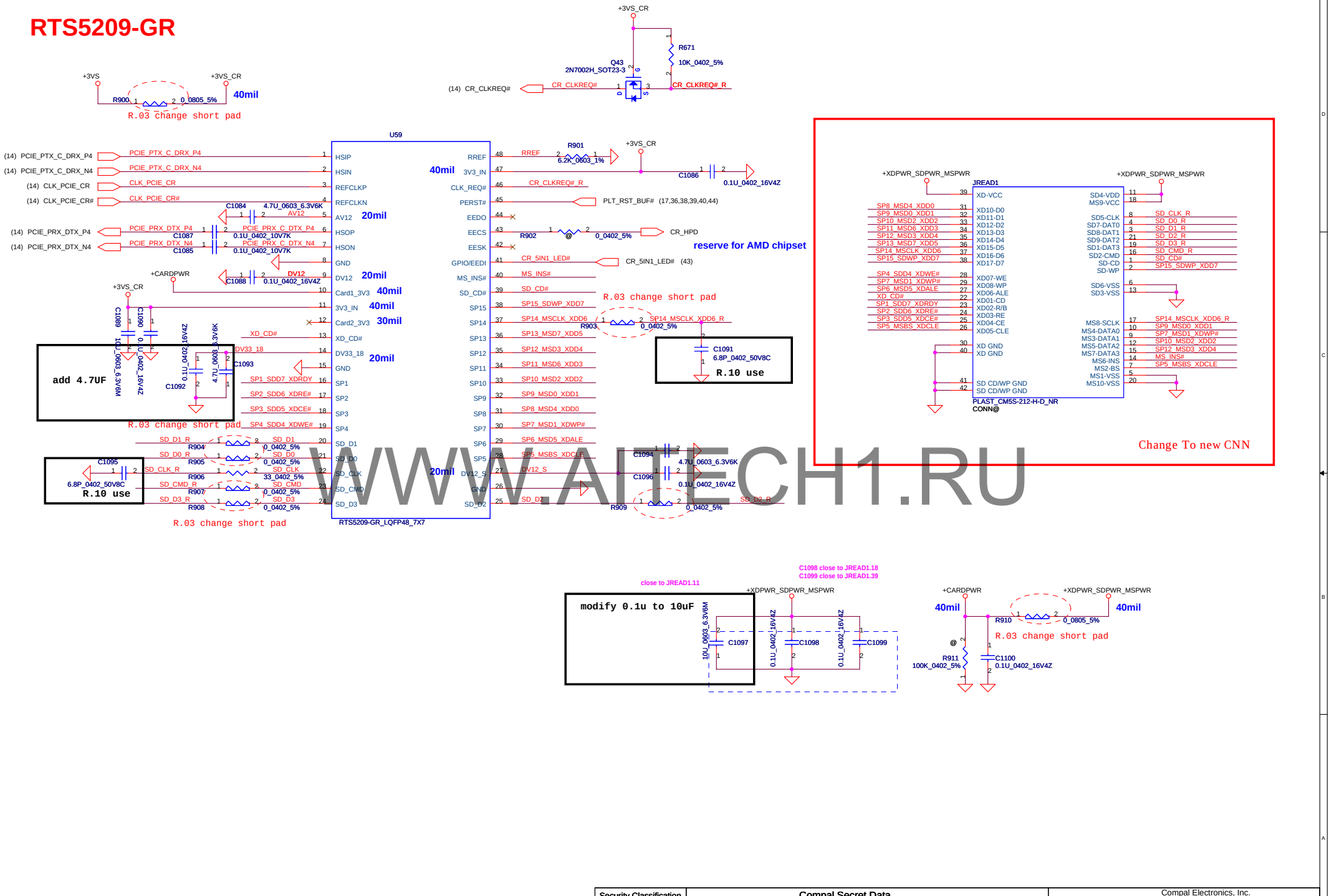
RTS5209-GR



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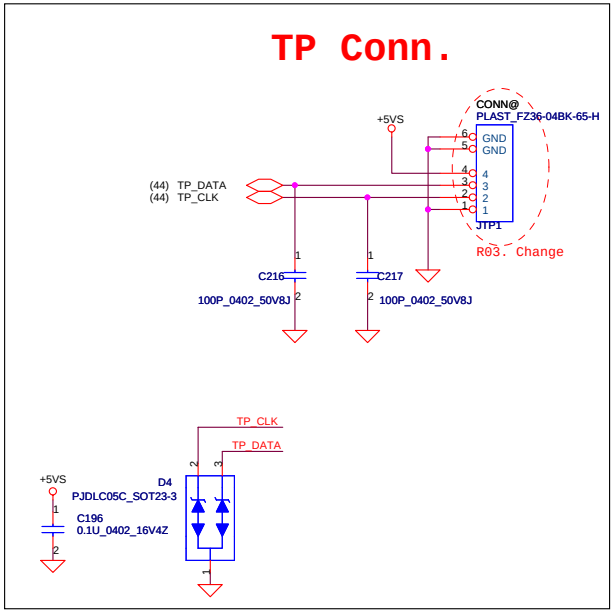
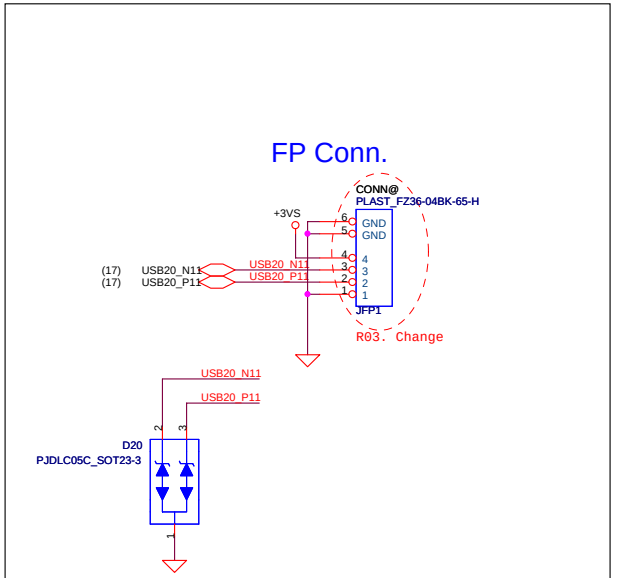
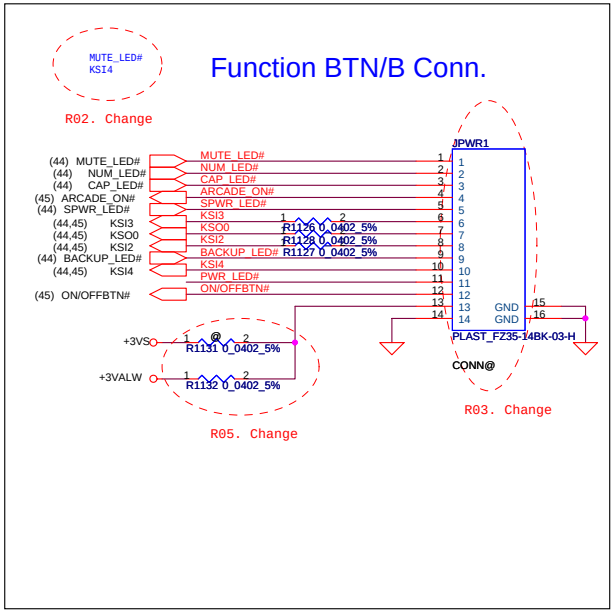
TP Conn.



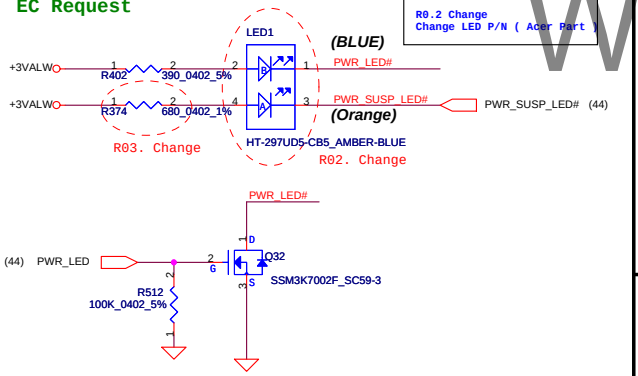
FP Conn.

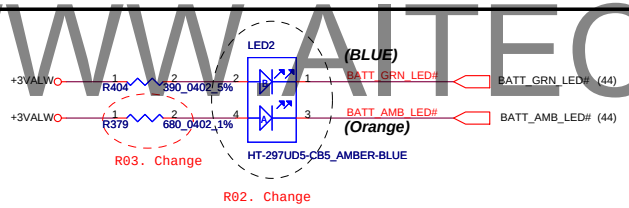


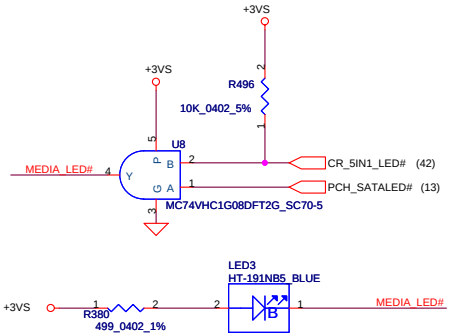
Function BTN/B Conn.

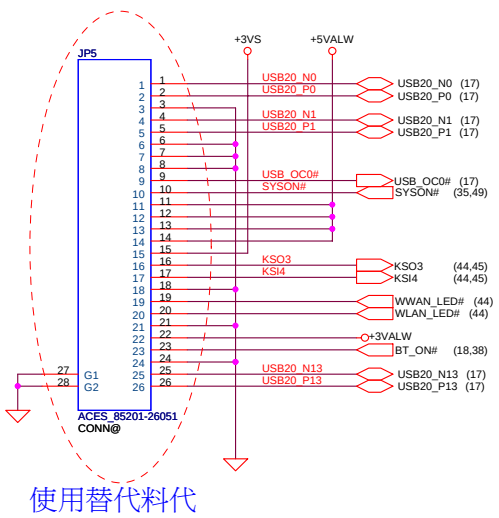


EC Request









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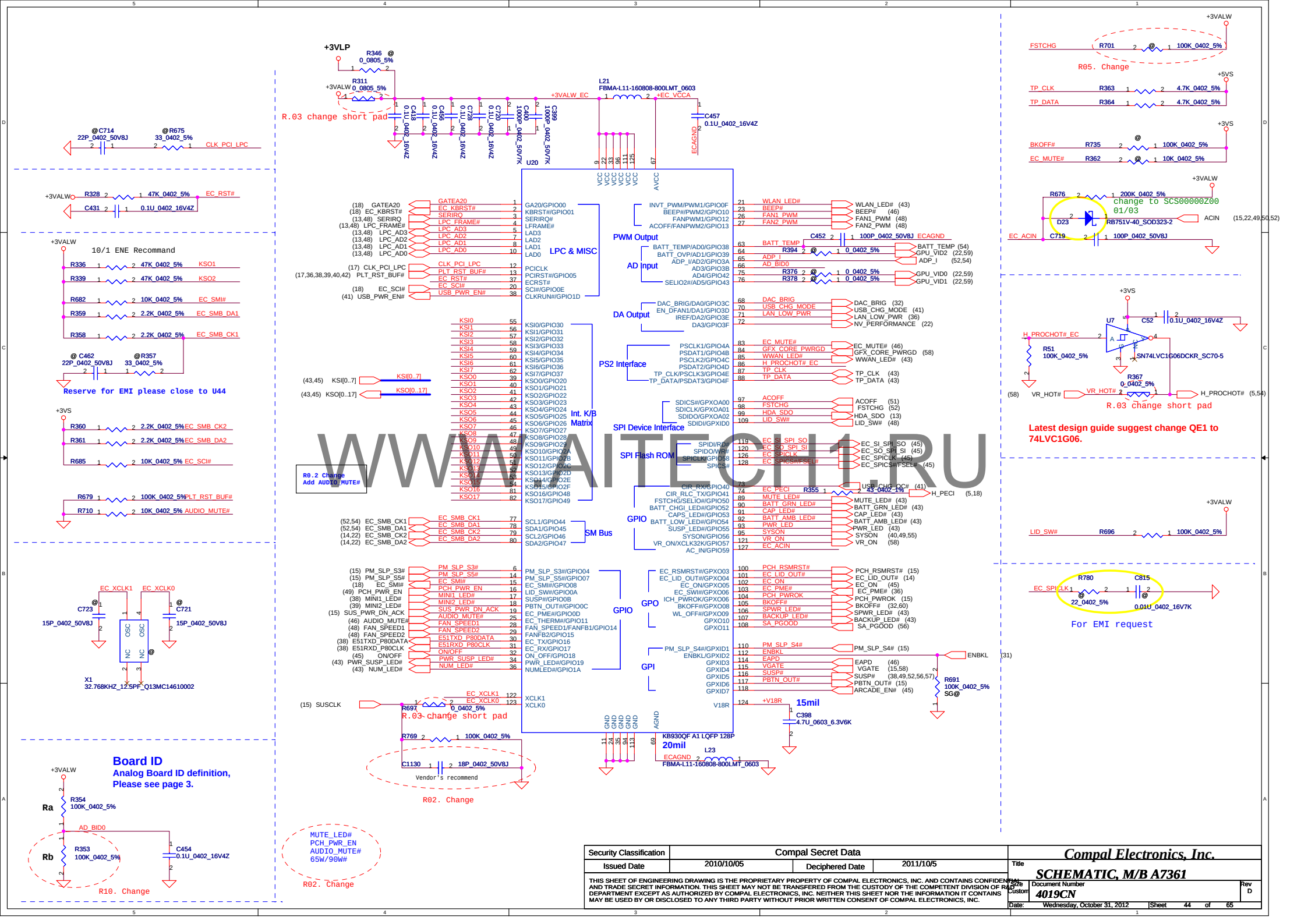

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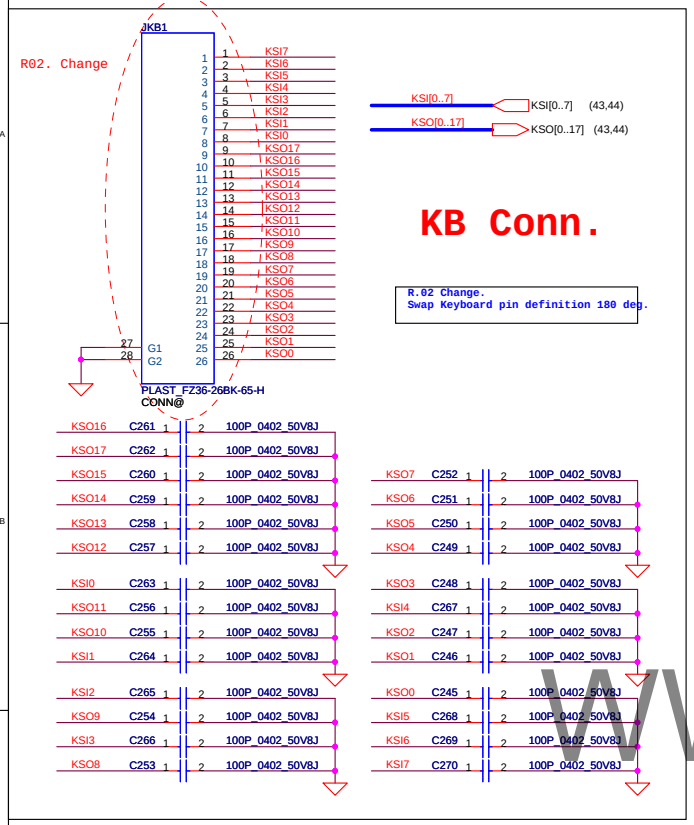

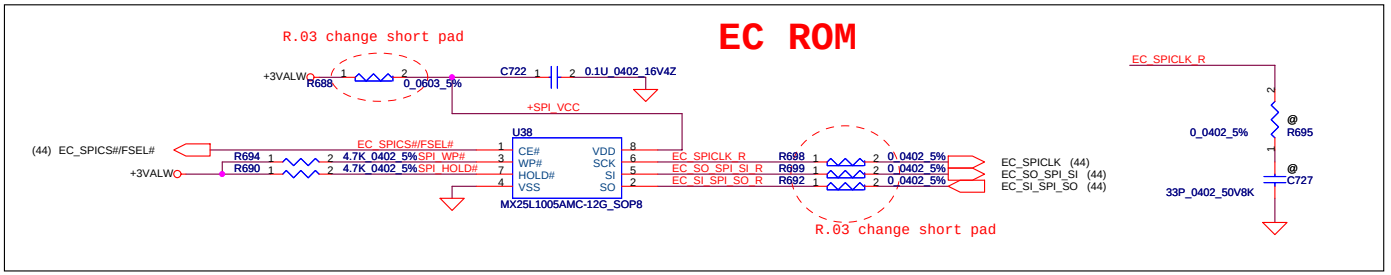

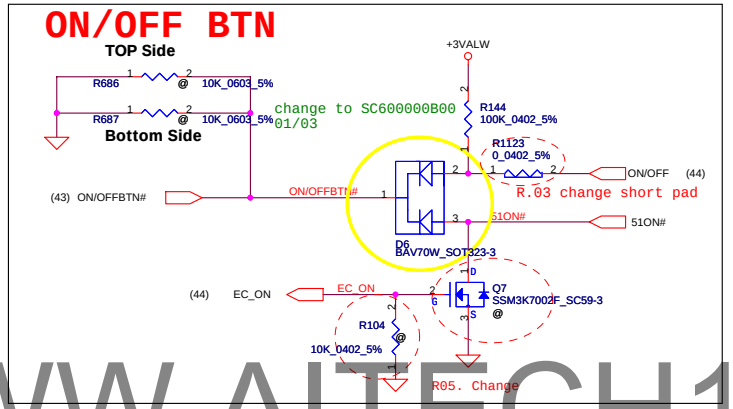

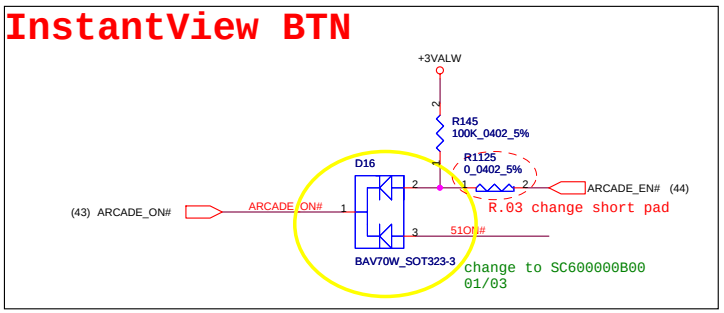

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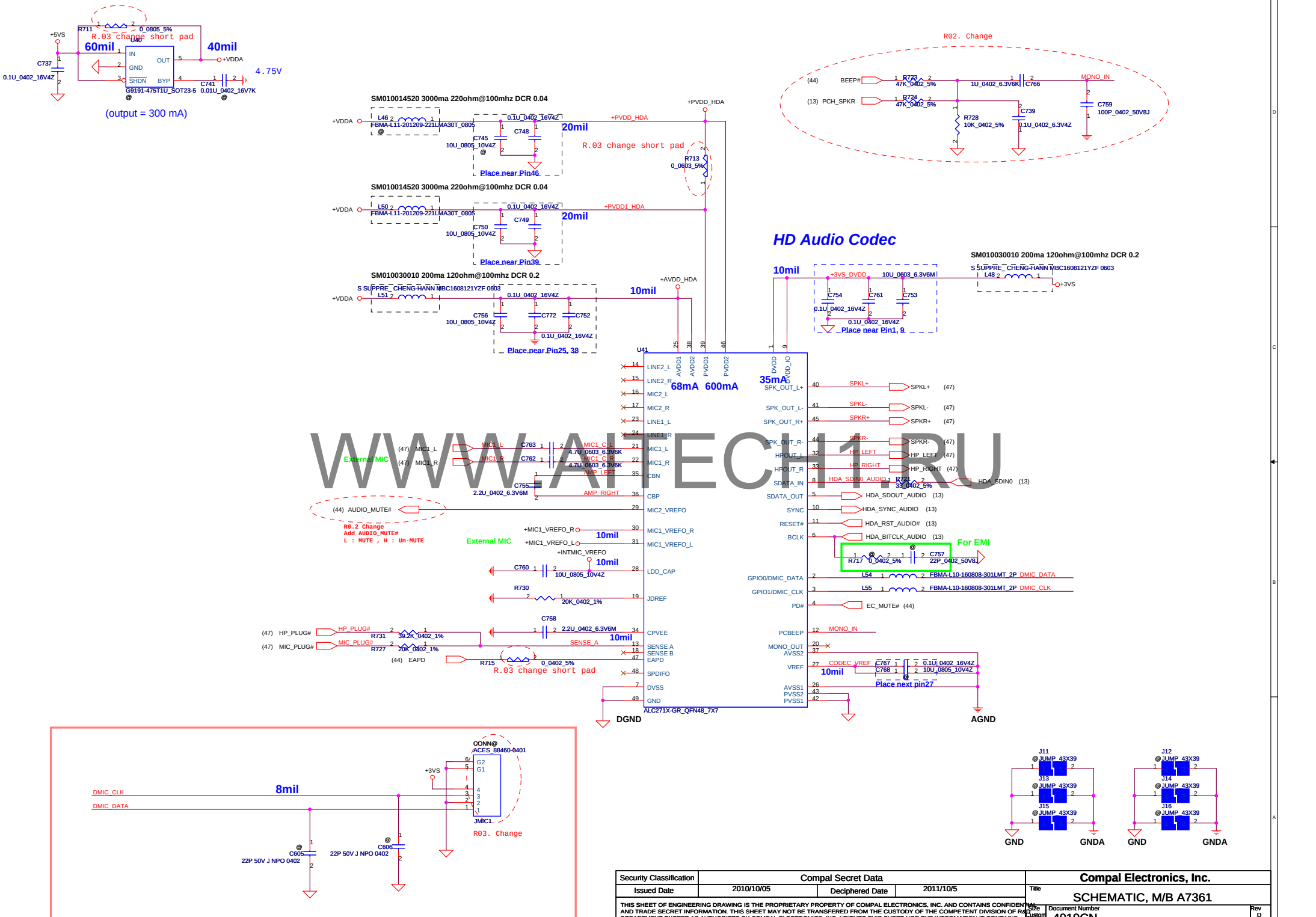

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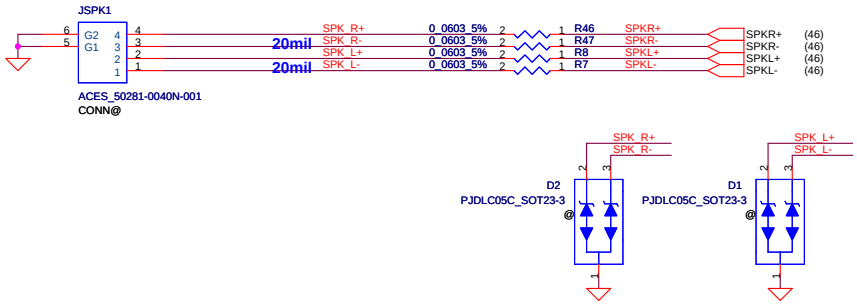
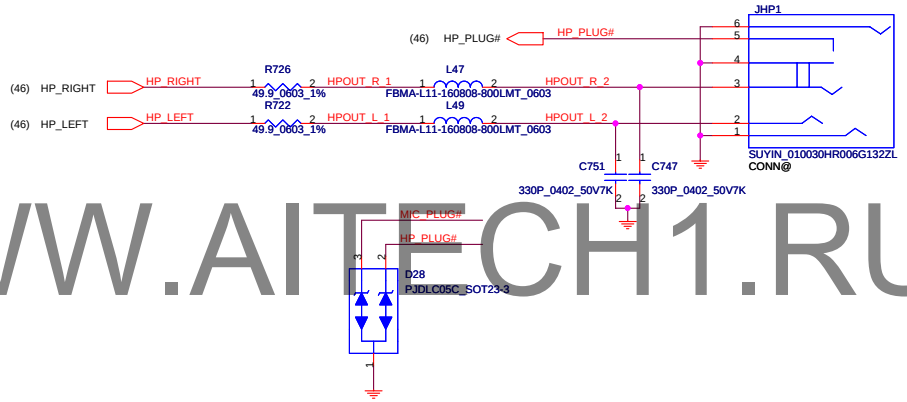
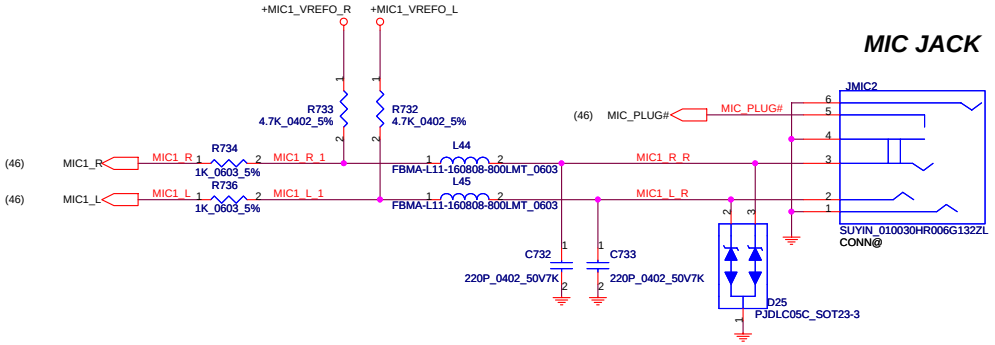
Int. Speaker Conn.



Headphone Out



MIC JACK



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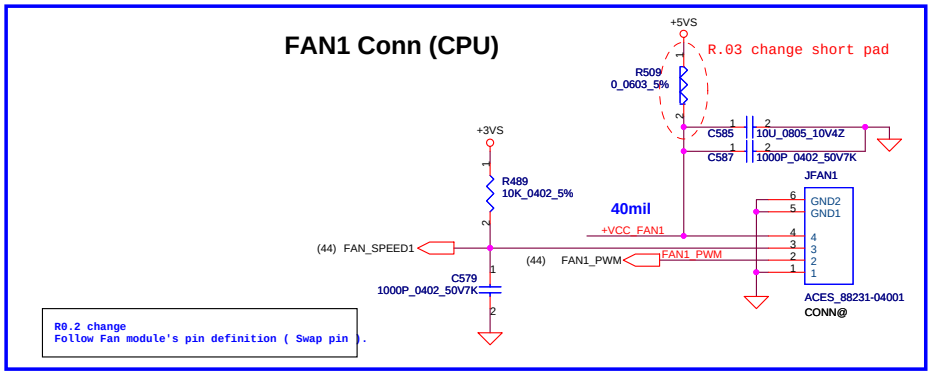
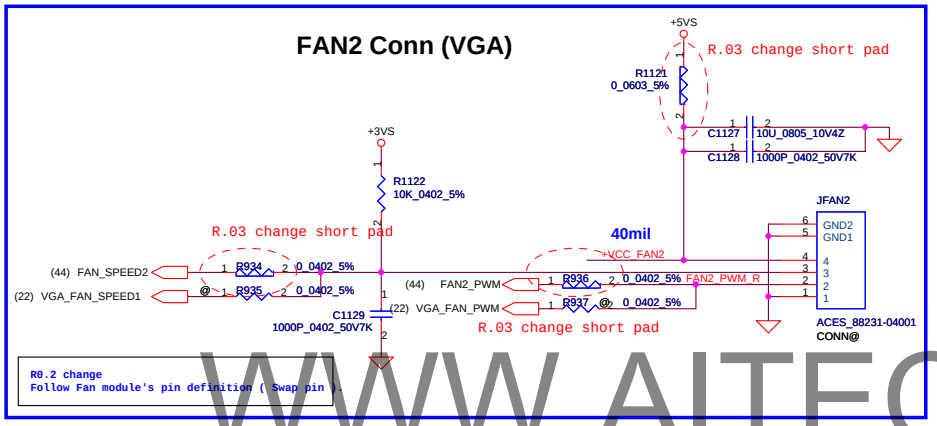
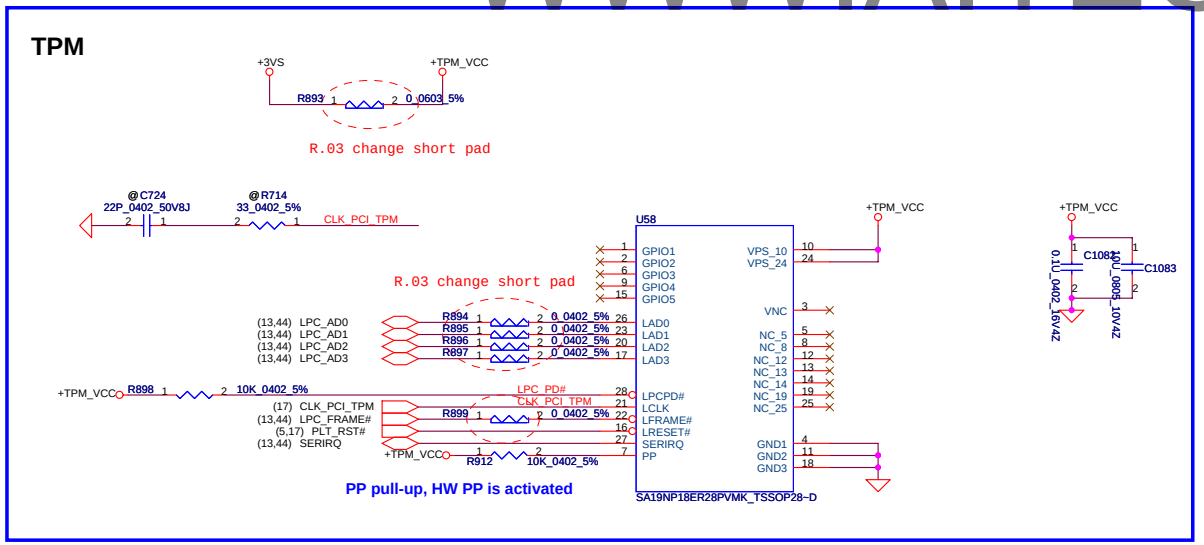
FAN1 Conn (CPU)



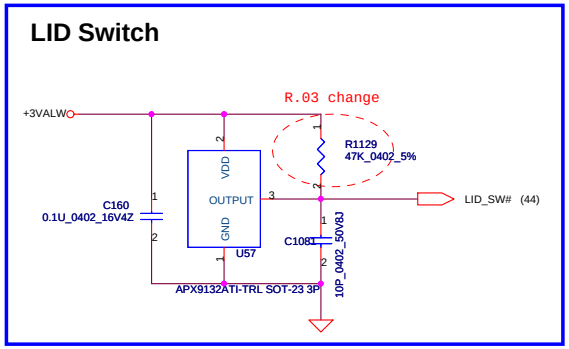
FAN2 Conn (VGA)



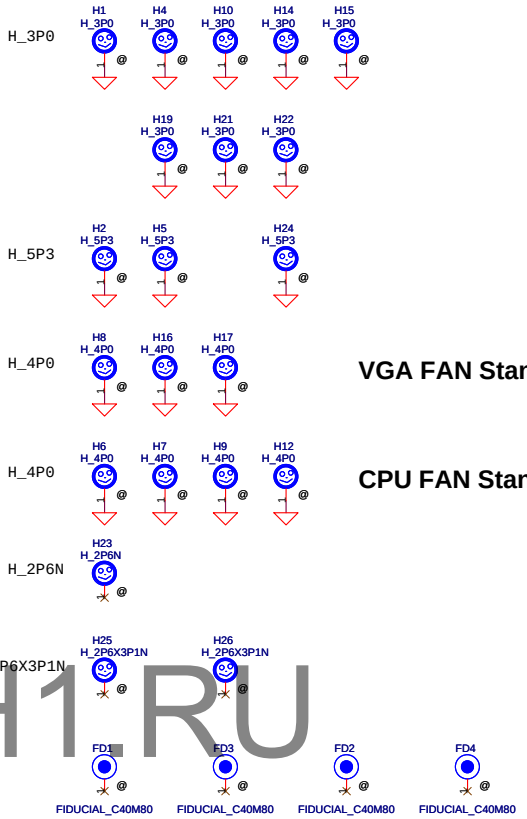
TPM



LID Switch



H_3P0 / H_5P3 / H_4P0 / H_2P6N / H_2P6X3P1N



VGA FAN Stand-Off

CPU FAN Stand-Off

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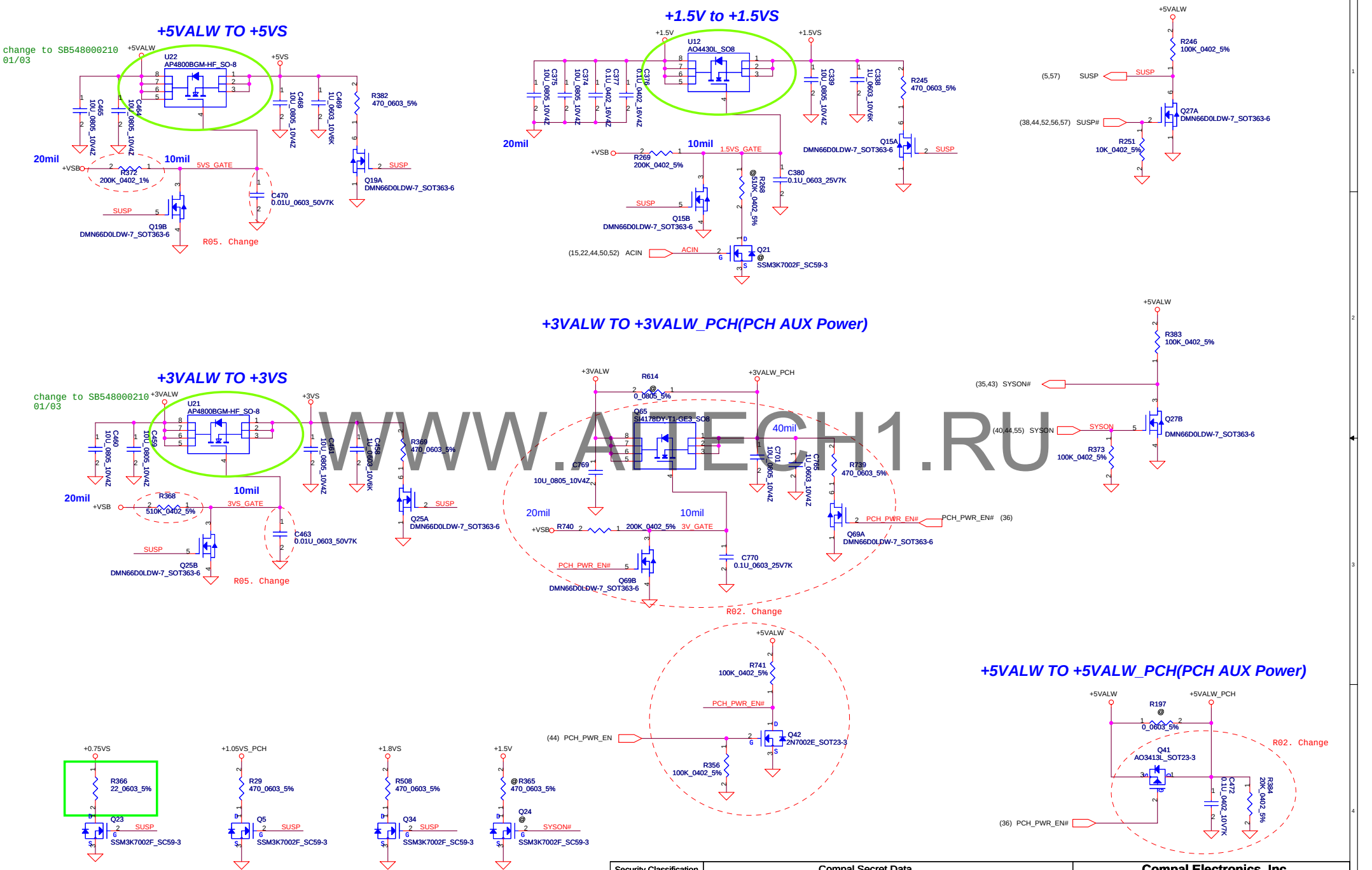

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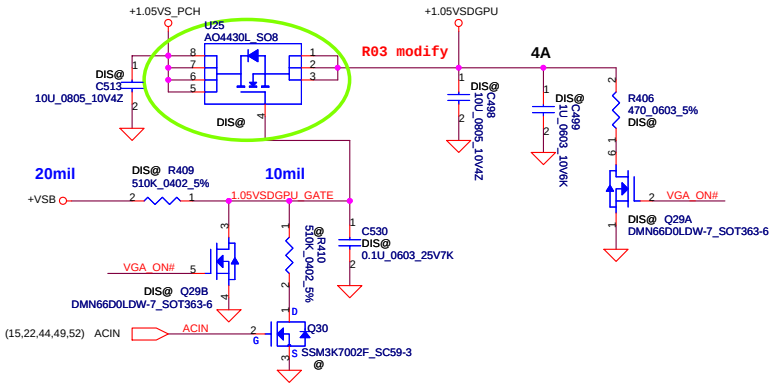
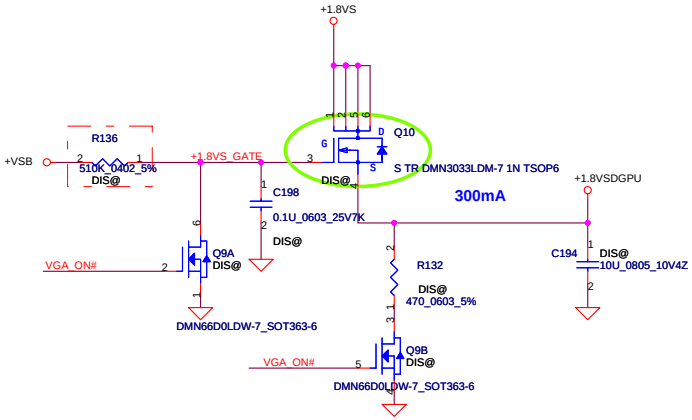
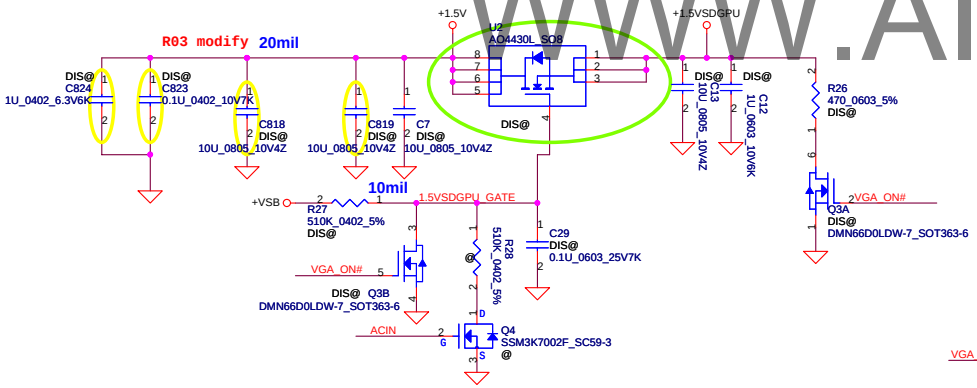
+1.05VS_VTT to +1.05VSDGPU for GPU



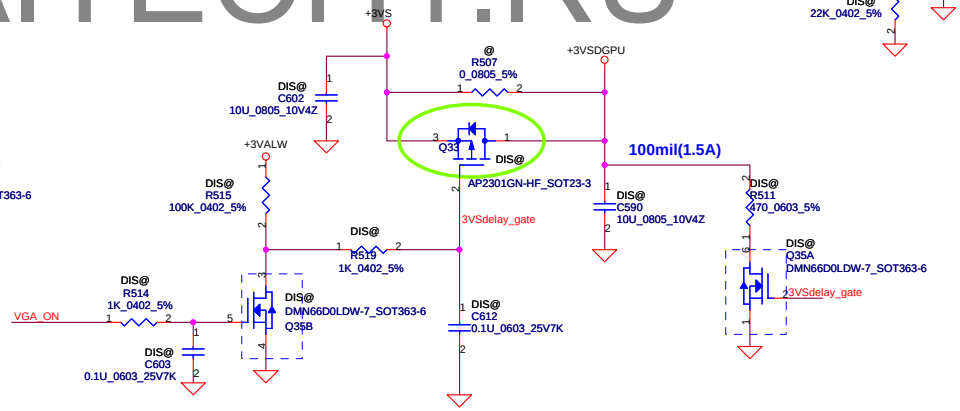
+1.8VS to +1.8VSDGPU for GPU

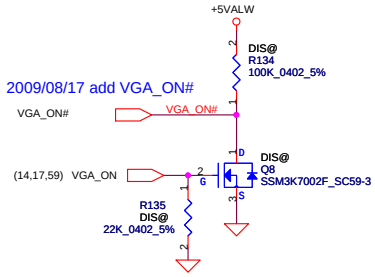


+1.5V to +1.5VSDGPU for GPU



+3VS to +3VSDGPU for GPU





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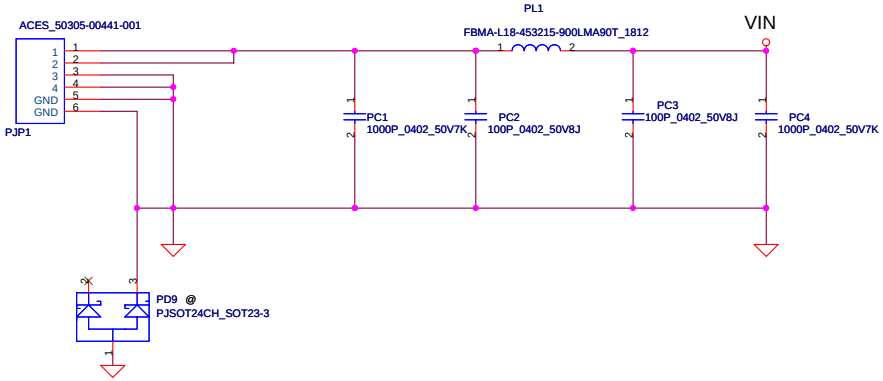

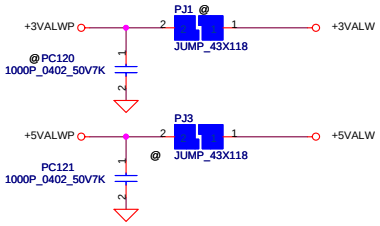

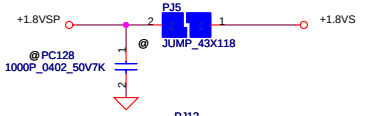

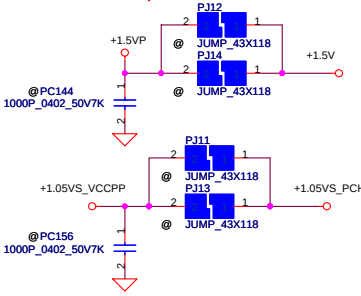

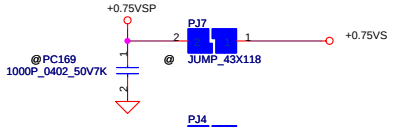

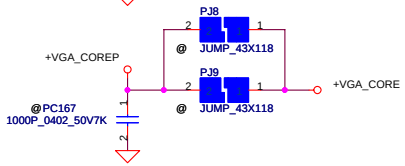

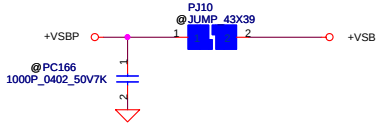

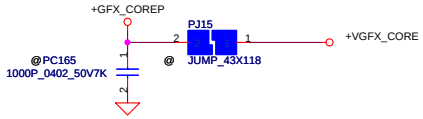

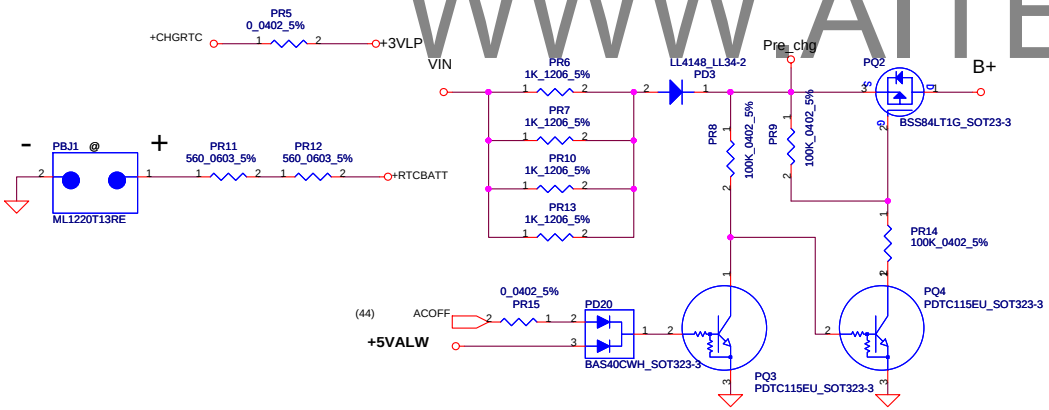

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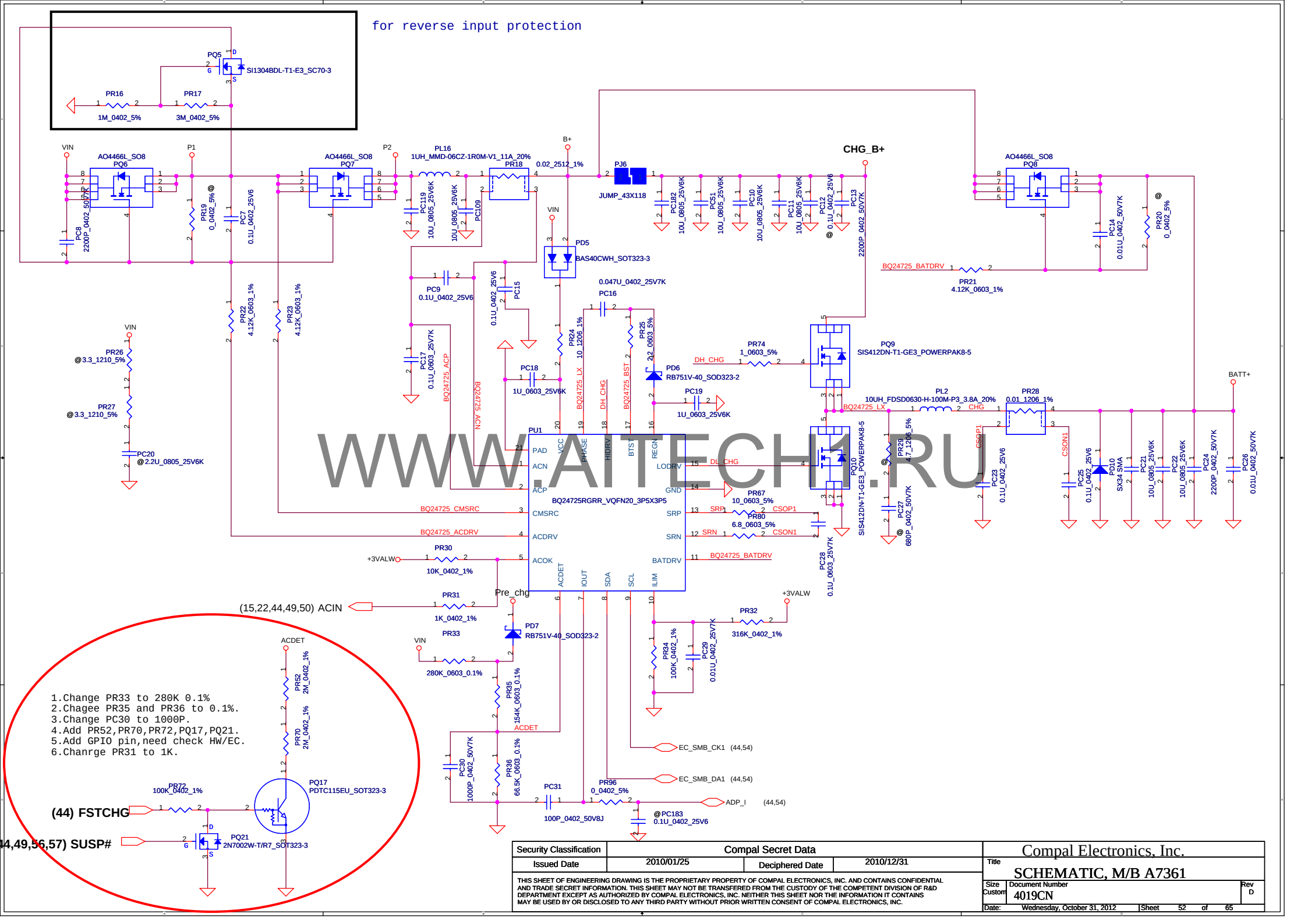

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Issued Date	2010/01/25	Deciphered Date	2010/12/31

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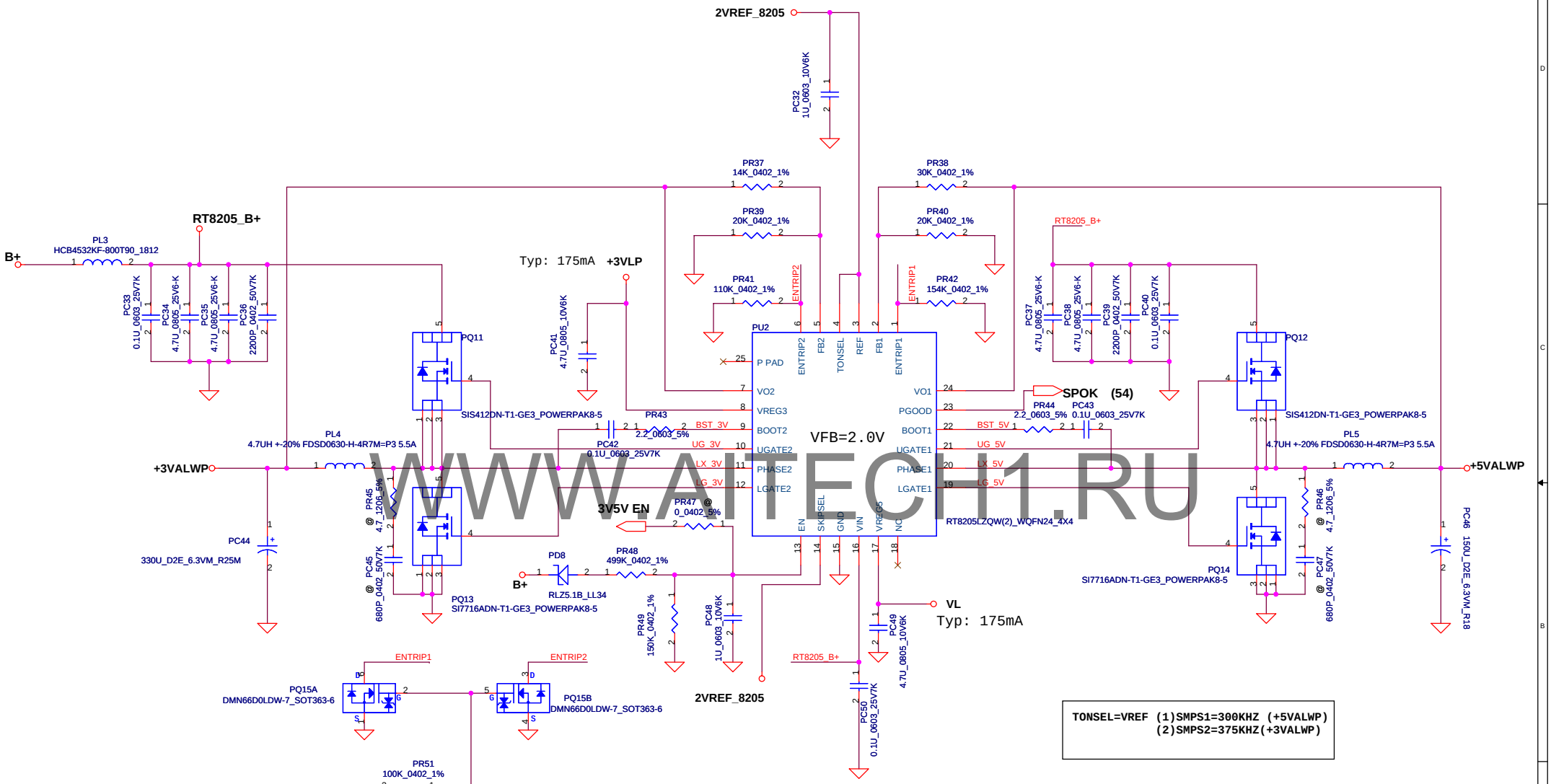

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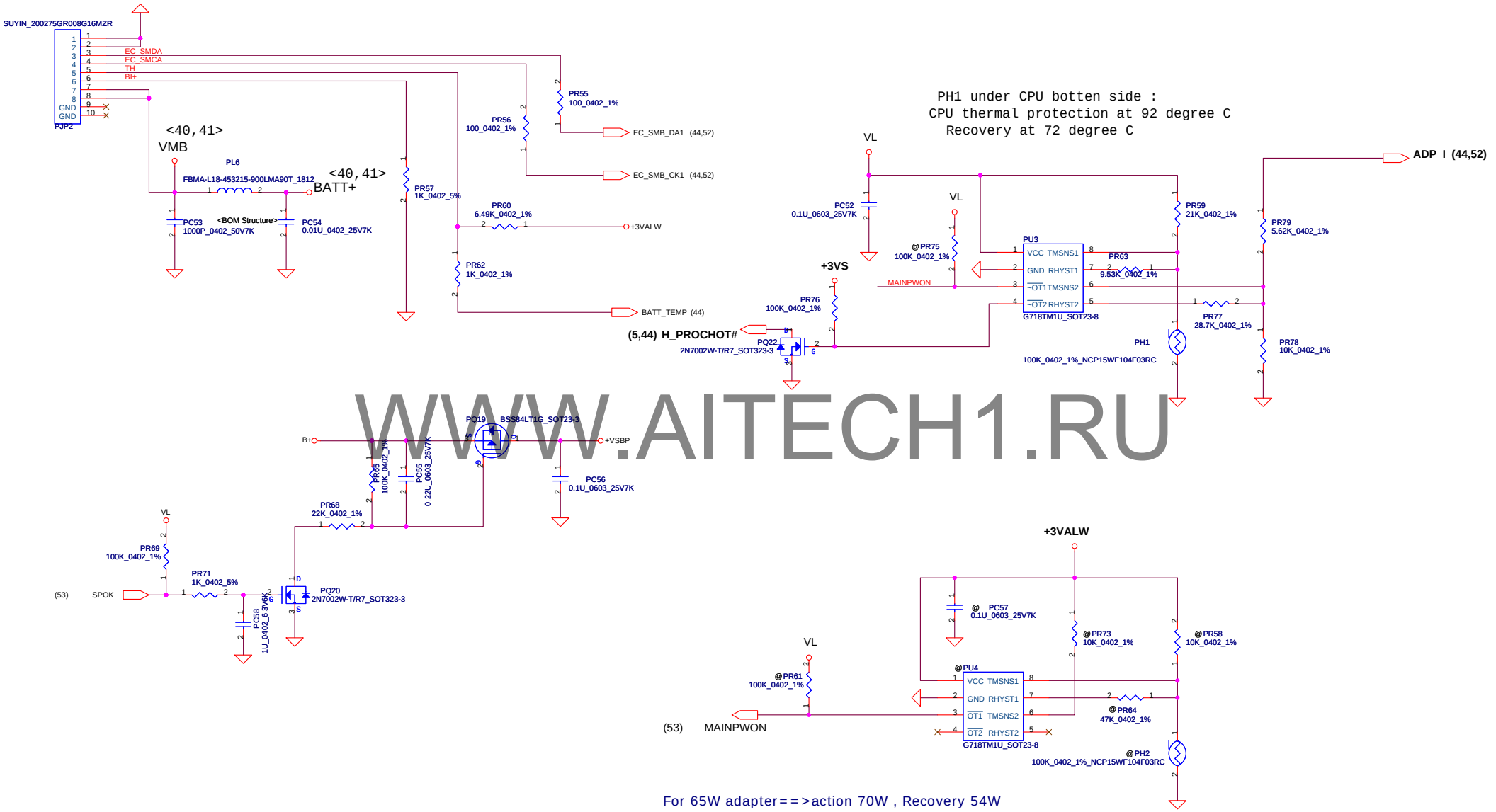

For 65W adapter==>action 70W , Recovery 54W

For 90W adapter==>action 97W , Recovery 75W

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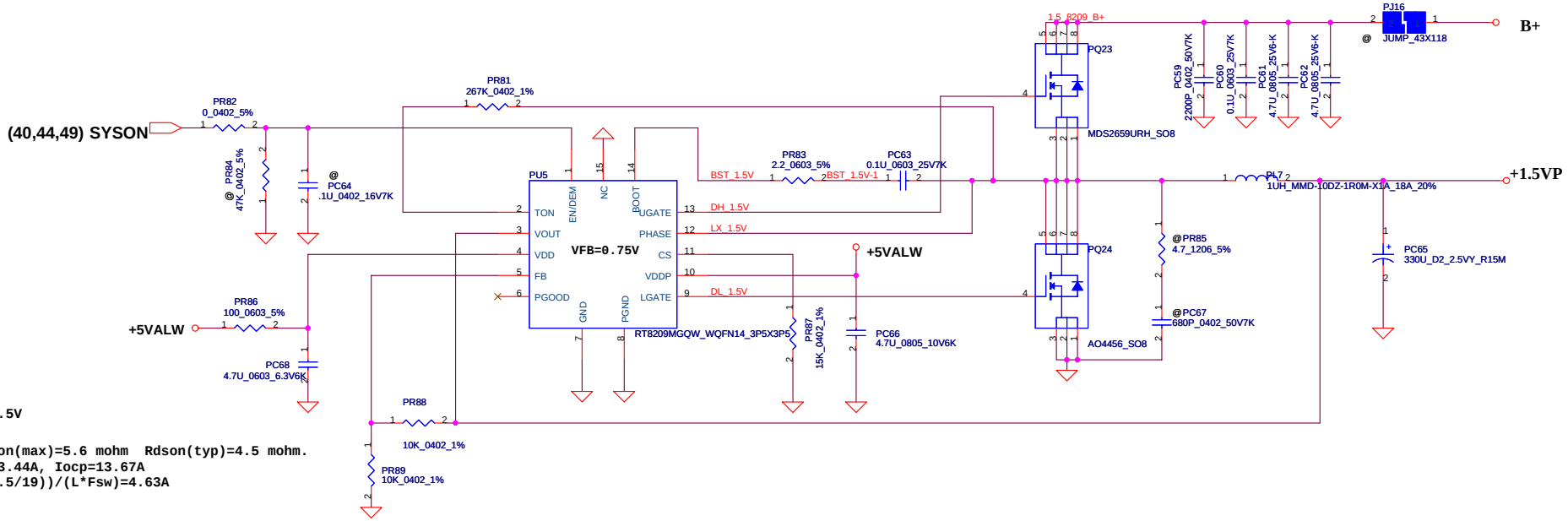

<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=19.53A, Imax=23.44A, Iocp=13.67A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+2.315A=35.65A
Iocpmin=((15K*9uA)/(0.0056*1.3))+2.315A=23.06A
Iocp=23.06A~35.65A

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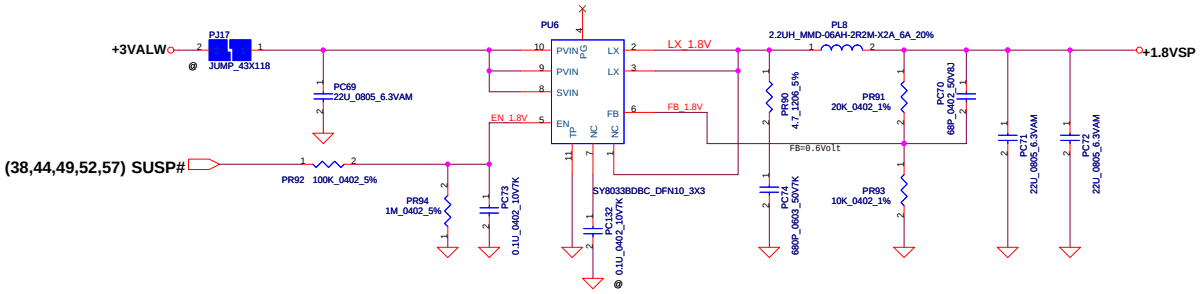
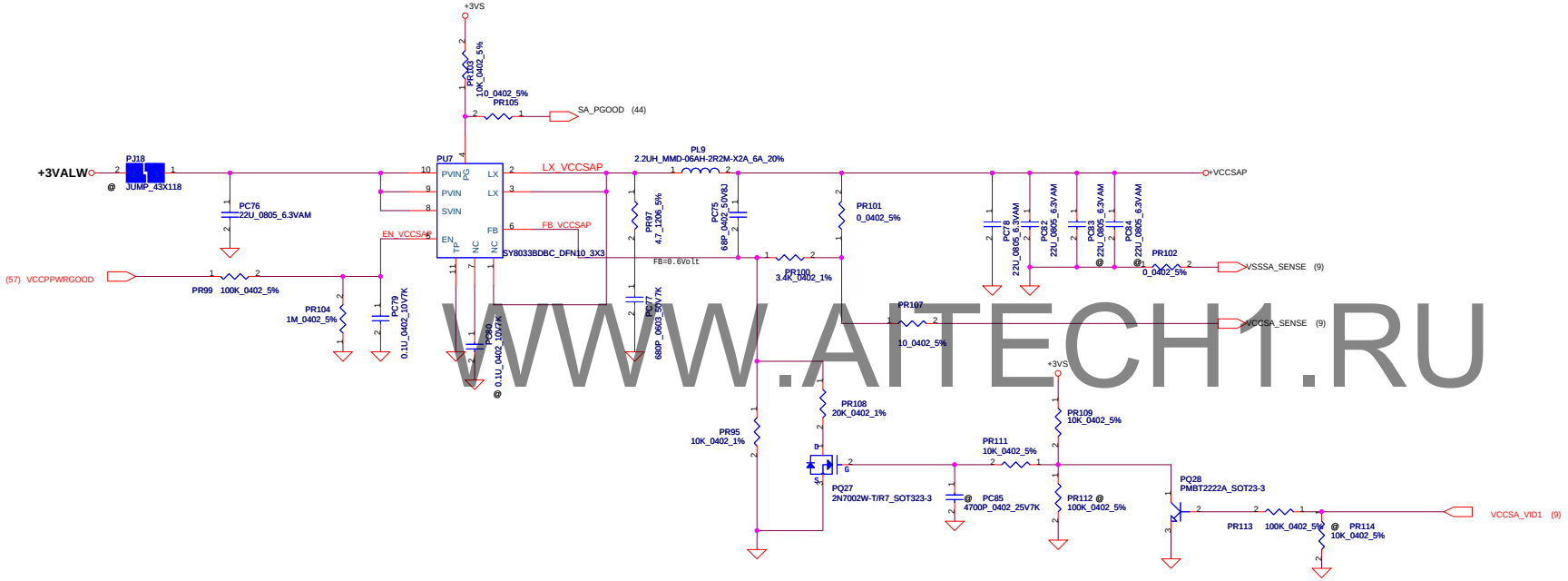
1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ;Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V





VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

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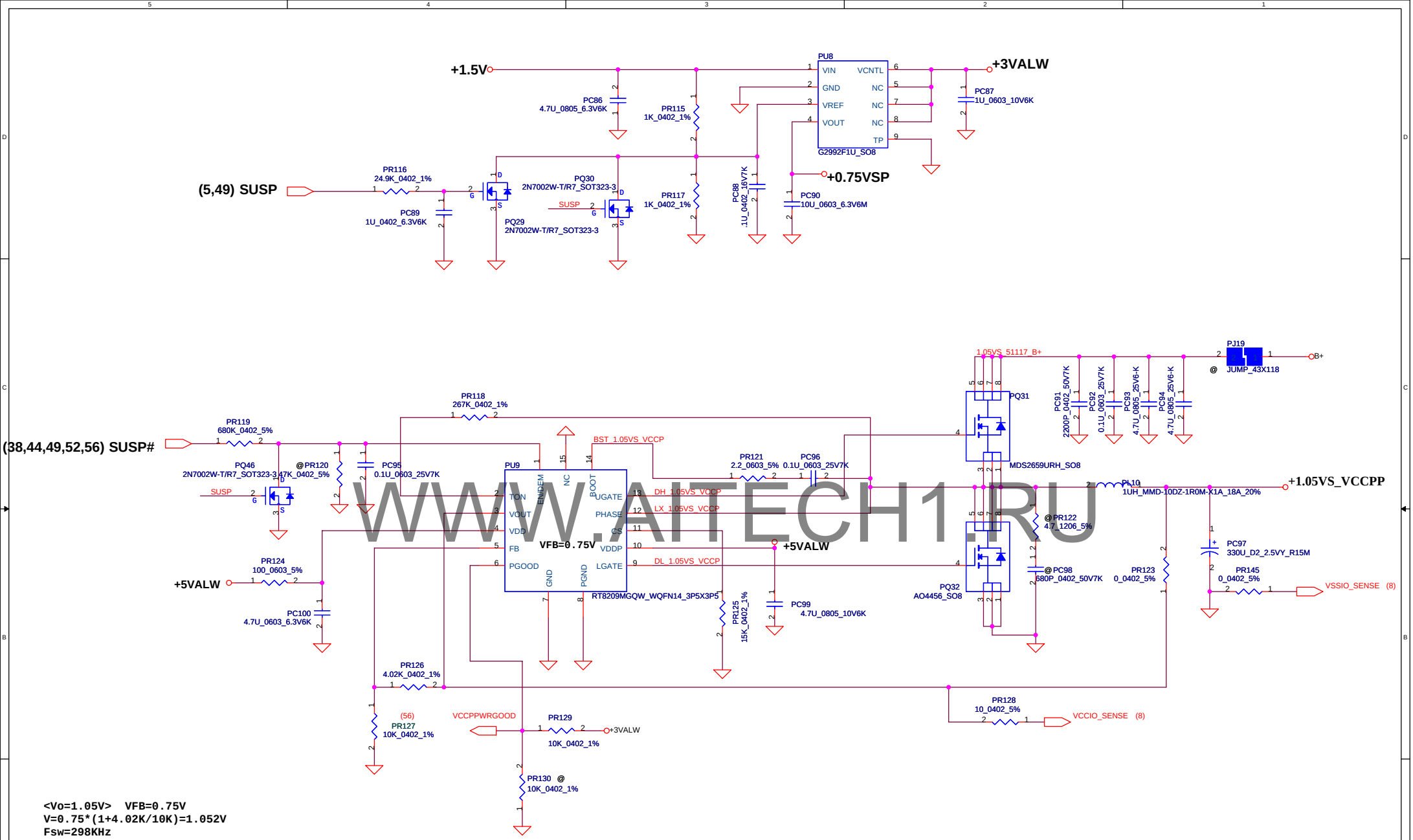

<Vo=1.05V> VFB=0.75V
V=0.75*(1+4.02K/10K)=1.052V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=12.866A, Imax=9A, Iocp=15.439A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.33A
=>1/2Delta I=1.665A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+1.665A=37.62A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=23.02A
Iocp=23.02A~37.62A

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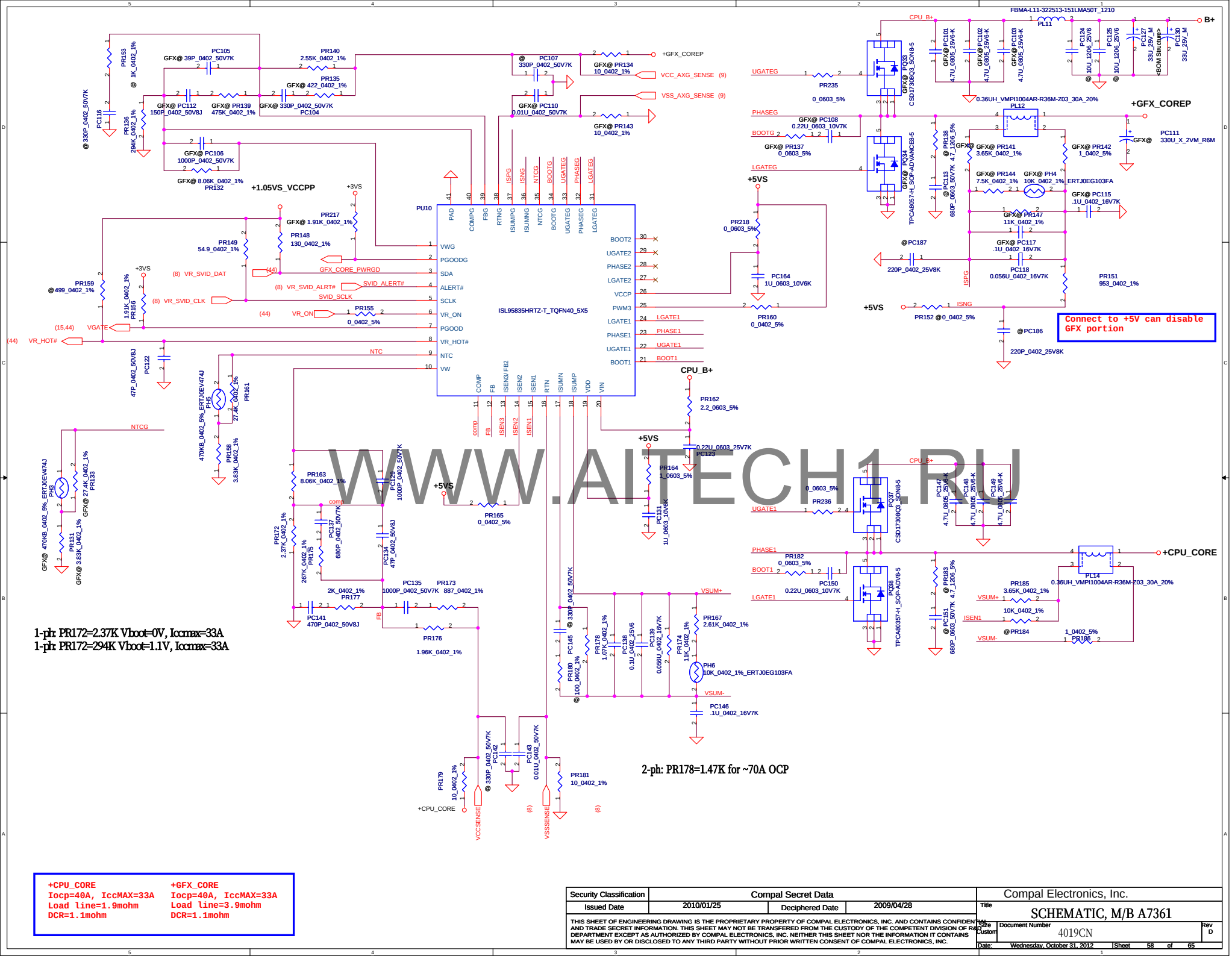

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Issued Date	2010/01/25	Deciphered Date	2009/04/28

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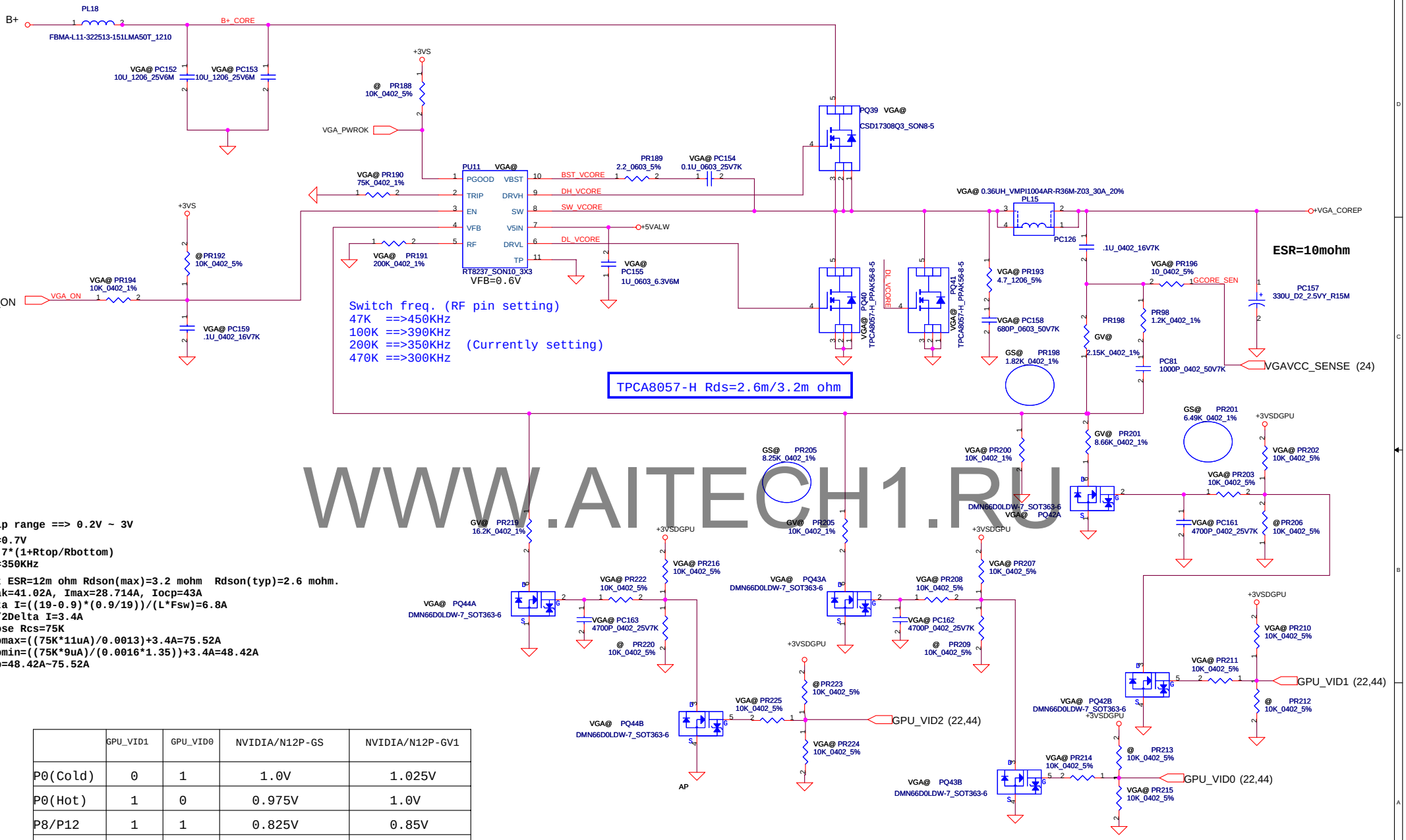

Vtrip range ==> 0.2V ~ 3V

VFB=0.7V
V=0.7*(1+Rtop/Rbottom)
Fsw=350KHz

Cout ESR=12m ohm Rdson(max)=3.2 mohm Rdson(typ)=2.6 mohm.
Ipeak=41.02A, Imax=28.714A, Iocp=43A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A
=>1/2Delta I=3.4A
choose Rcs=75K
Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A
Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A
Iocp=48.42A~75.52A

	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P0(Cold)	0	1	1.0V	1.025V
P0(Hot)	1	0	0.975V	1.0V
P8/P12	1	1	0.825V	0.85V
ES	----	----	----	0.925V

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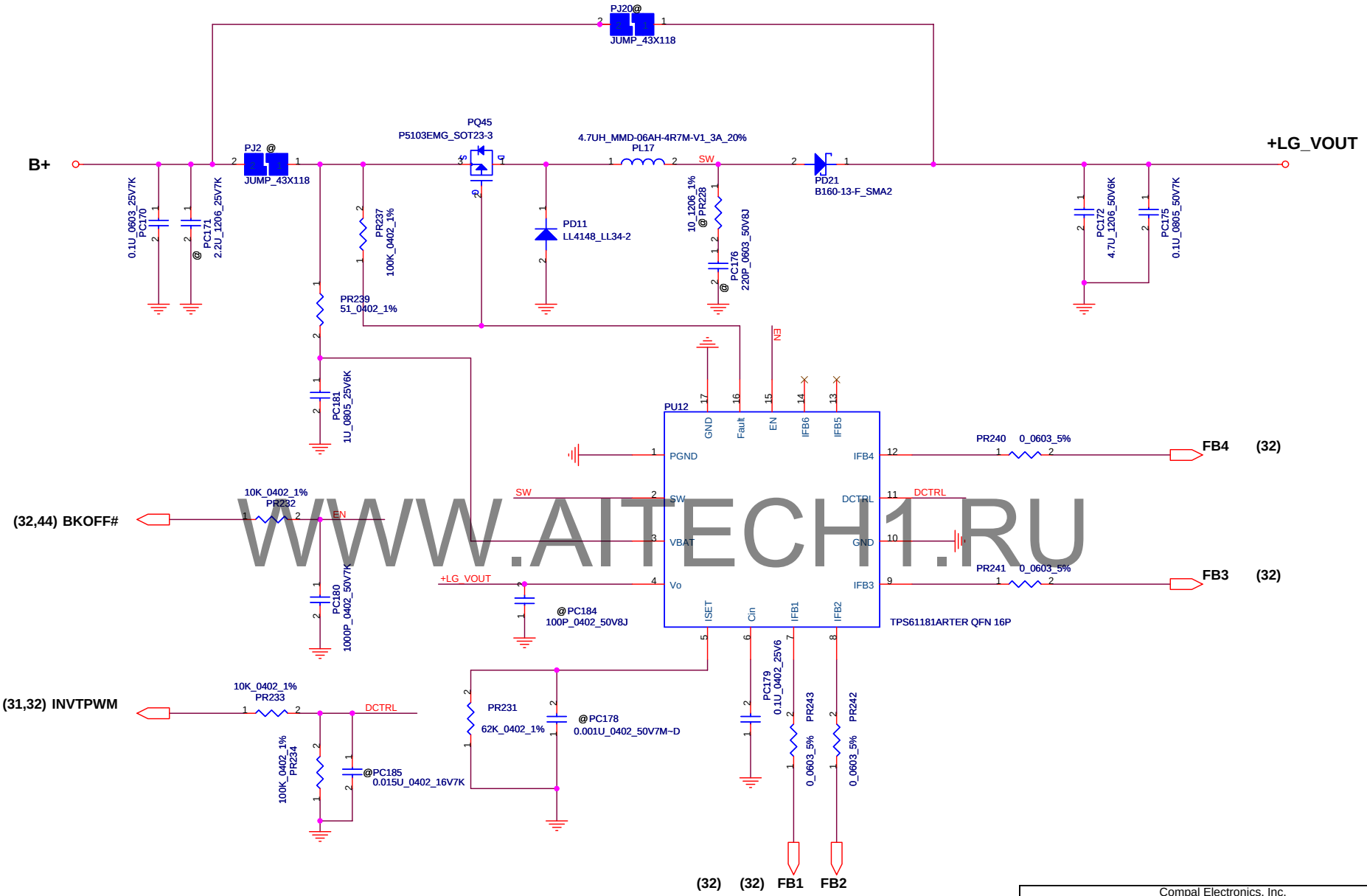

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PL16 from SH00000AQ00(有鹵) to SH00000MZ00(無鹵)	for PUR request	0.1	---	Change PL16 from SH00000AQ00 to SH00000MZ00	2010/12/29	
2	Change component from PR52 to JUMP20	Reservation two state and cost down for panel driver system	0.1	---	Change component from PR52 to JUMP20	2010/12/29	
3	ISN test fail	ISN solution			Change PL16 to 1uH PL2 to 10UH	2011/02/08	
4	Costdown				PU3 circuit merged with PU4 circuit	2011/02/08	
5	Add PR74=1 ohm	EMI solution			Add PR74=1 ohm	2011/02/08	
6	Add PD10	To restrain Battery surge current		---	Add PD10	2011/02/08	
7	change Shuriken LED driver circuit	for lower cost design		---	change PU12 Shuriken LED driver circuit	2011/02/16	
8	change GFX OCP	for auto restart issue		---	Change PR151 from 619 to 953	2011/05/13	PVT2
9	change GFX Loadline	for auto restart issue		---	Change PR140 from 1.69K to 2.55K	2011/05/13	PVT2
10	PR184 to be removed, because of 1-phase	for auto restart issue		---	Delete PR184	2011/05/13	PVT2
11	Change PC95 from 4.7uF to 0.1uF	for instantView boot time		---	Change PC95 from 4.7uF to 0.1uF	2011/05/13	PVT2
12	Change PQ23,PQ31 from AO4406AL to MDS2659URH	CPU damage issue			Change PQ23,PQ31 from AO4406AL to MDS2659URH	2011/05/13	PVT2
13							
14							
15							

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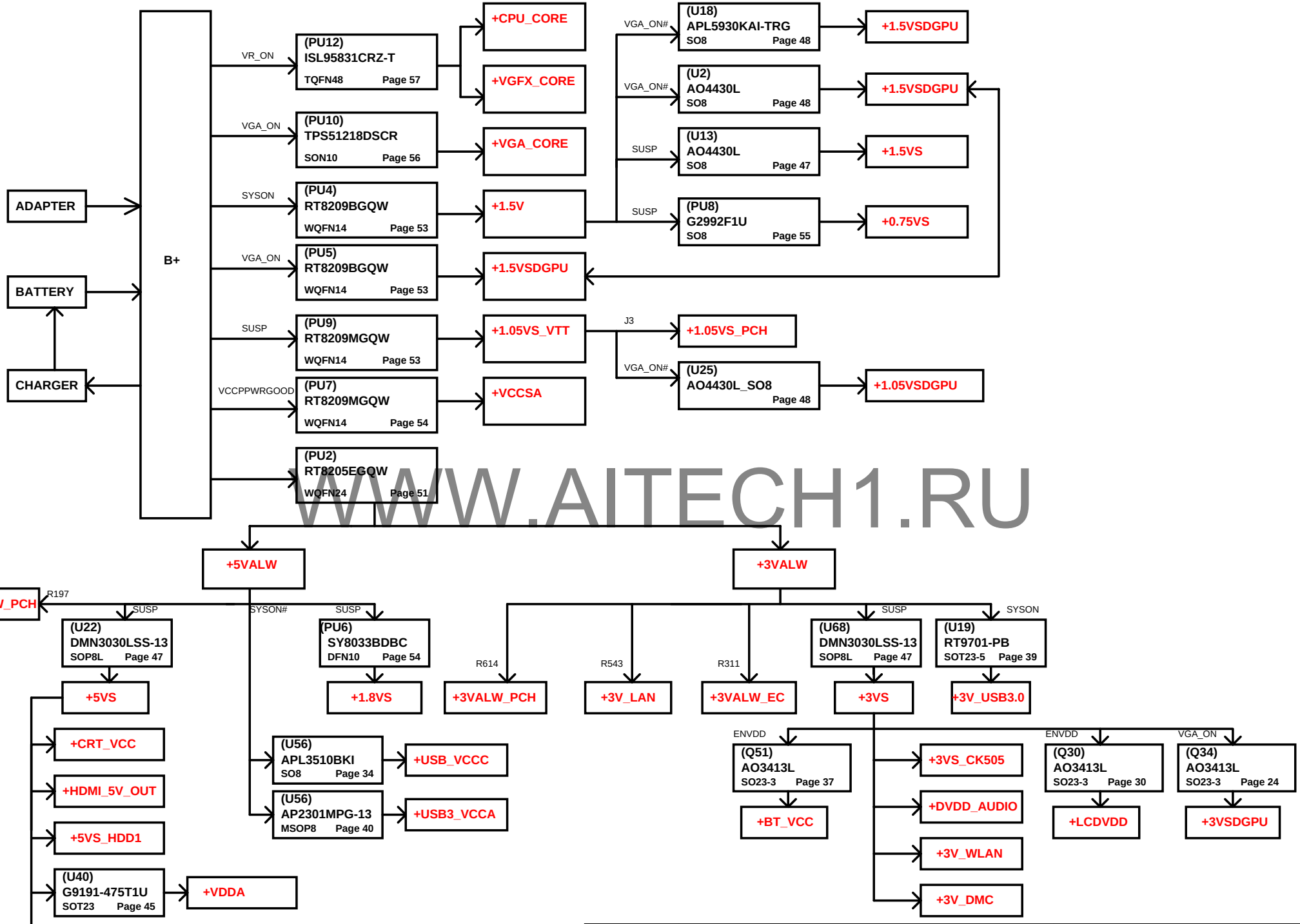

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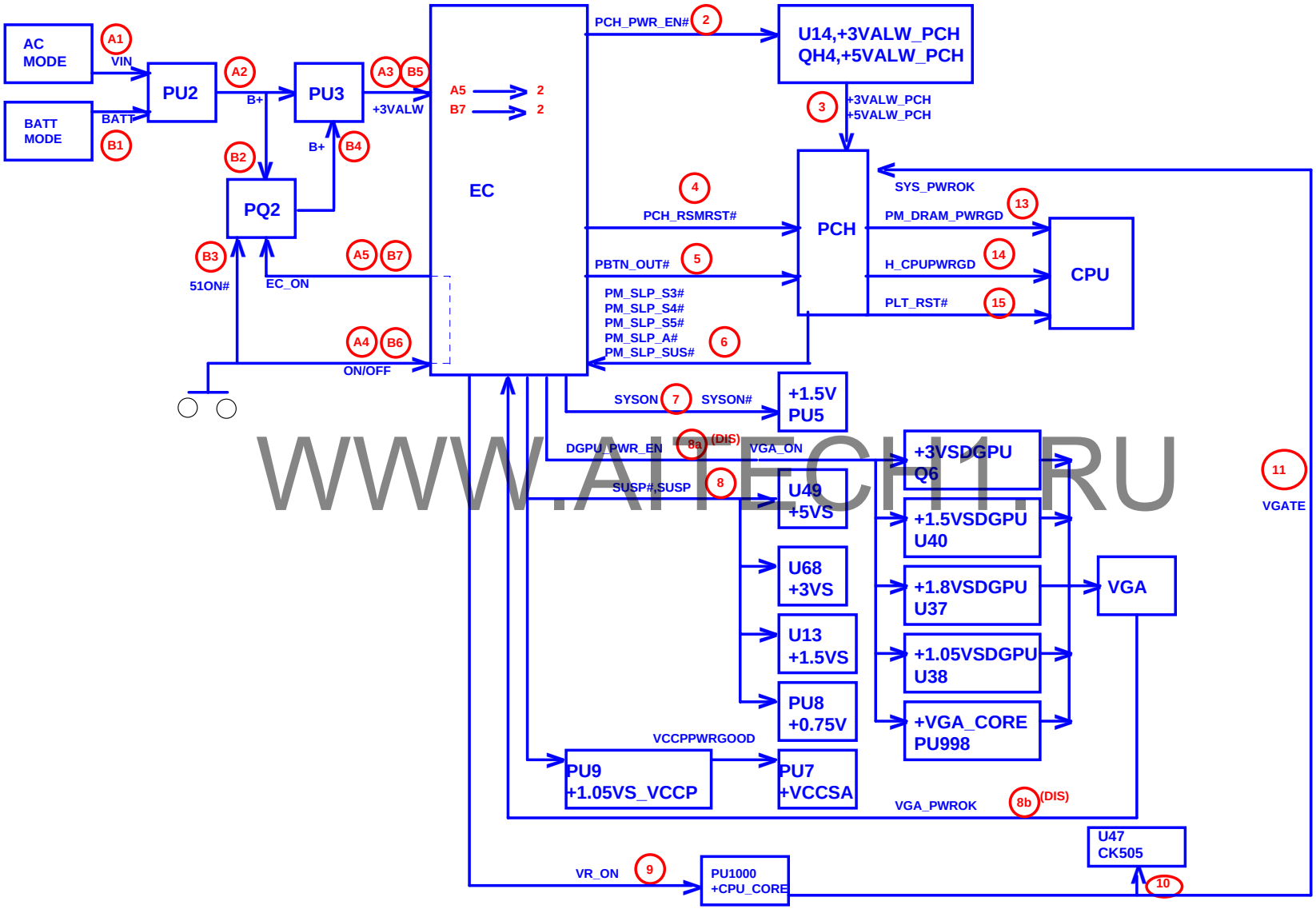

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.45	Keyboard connector	2011.02.18	ME	For KB's assembly issue, Reverse connector to 180°	Reverse JKB1 to 180°	R0.2
2	P.35	ESATA re-driver IC	:	HW	RX's signal is incorrect.	Modify circuit, change INPUT side to OUTPUT side.	:
3	P.35	Interference	:	ME	Capacitor C989 has risk to short thermal module.	Re-placement C989	:
4	P.39	Interference	:	ME	JMINI2's upside component interfere C cover.	Re-placement JMINI2's upside component	:
5	P.34	Interference	:	ME	Q13,Q14 interfere C cover	Re-placement Q13, Q14	:
6	P.48	CPU & VGA FAN connector	:	HW	Pin definition need follow module design rule.	swap JFAN1's & JFAN2's pin.	:
7	P.48	USB3.0 charger LED	:	HW	Follow Customer's requirment.	Delete LED4 , cancel USB chargeing button design	:
8	P.48	LED indicator	:	HW	LED's pin is reverse.	Change LED1,LED2 to genernal part.	:
9	P.47	HP Jack, MIC Jack	:	ME	Base on ID, HP & MIC jack are reverse.	Follow ID design, swap JHP1, JMIC2 jack.	:
10	P.13	Audio HDA signal	:	HW	HDA's SYNC need imrpve component side signal quality.	Meet Intel design guide, change isolate MOSFET (Q36) voltage to +5VS	:
11	P.20	Component interference	:	HW	Capacitor's highness over ME's SPEC (>1.5mm)	Change C278, C279 to 1.4mm	:
12	P.37	LCM cable assembly	:	DFX	LCM cable assembly issue	For LCM cable assembly, move C618/C619/C620 to BOT side	:
13	P.37	Lan signal quality	:	HW	(IEEE) Giga LAN's CM voltage over SPEC (>50mV)	left GND via (driver IC) to reduce noise.	:
14	P.37	ID issue	:	ME	old RJ45 can't meet cusotmer ID requirement	Change a new RJ45 connector	:
15		RF reserves solution	:	RF	RF needs reserve soluiton	Add C1130, C1131, C1132, C1133, C1134, C1135 and C1136 PAD.	:
16	P.49	PCH power rail	:	HW	DC mode power consumption is over. (Support USB chargeing)	co-lay MOS at PCH's +5VALW_PCH / +3VALW_PCH, controlled by EC.	:
17	P.14	PCIE port colay	:	SW	SW need support turn off LAN function by BIOS menu	co-lay Port1 & Port6 for on board LAN	:
18	P.46	Audio PC BEEP	:	HW	PC BEEP circuit is not latest module design	Follow module design & cost down	:
19	P.46	MIC MUTE function	:	Customer	Base on customer requirment add MIC mute function	Change Audio Codec pin 29 as GPIO, connect to EC	:
20	P.14	ASF function	:	HW	ASF function isn't workable	Co-lay PCH's SMBUS channel for ASF2.0	:
21	P.36	LAN Power rail	:	HW	LAN's power need turn off at DC mode	co-lay MOS at PCH's +3V_LAN, controlled by EC.	:
22	P.40	USB3.0 Power leakage	:	HW	USB3.0 power leakage issue	Add MOS(Q45,Q50) at USB30_SMI/CLKREQ_USB3 to prevent leakage issue.	:
23		Non-colay 0 ohm change to short pad	2011.03.29	HW	Non-colay 0 ohm change to short pad		R0.3
24	P.13	Change BIOS ROM	:	HW	SW need support Dual output BIOS code	Change dual output ROM	:
25	P.18	DGPU_PWROK	:	HW	common design for DGPU_PWROK	change use mos to control	:
26	P.33	CRT filter	:	HW	short one filter to reduce DAC overshoot	Change L28、L30、L33 to 0 ohm.	:

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23	P.43	Connector	2011.03.29	ME	DFX highlight connector issue	Change TP、FP、BTN connector	R0.3
24	P.32	Connector	:	HW	DFX highlight assemble issue	Change LVDS pin define, avoid PWR & GND near	:
25	P.48	Hall sensor	:	HW	Change hall sensor	Add a pull high for new part output	:
26	P.58	PWR noise	2011.04.08	PWR	PWR noise	Add PC130 & PC127	R0.4
27	P.24	NV VGA GND reference	2011.04.13	HW	NV VGA GND reference	Add R517	R0.5
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